ICAC

Workshop on IC Advances in China (ICAC)

A Fully Dynamic Low-Power Wideband Time-Interleaved Noise-Shaping SAR ADC

Haoyu Zhuang[1] and Nan Sun[2]

[1]University of Electronic Science and Technology of China, Chengdu, China

[2]Tsinghua University, Beijing, China

Outline

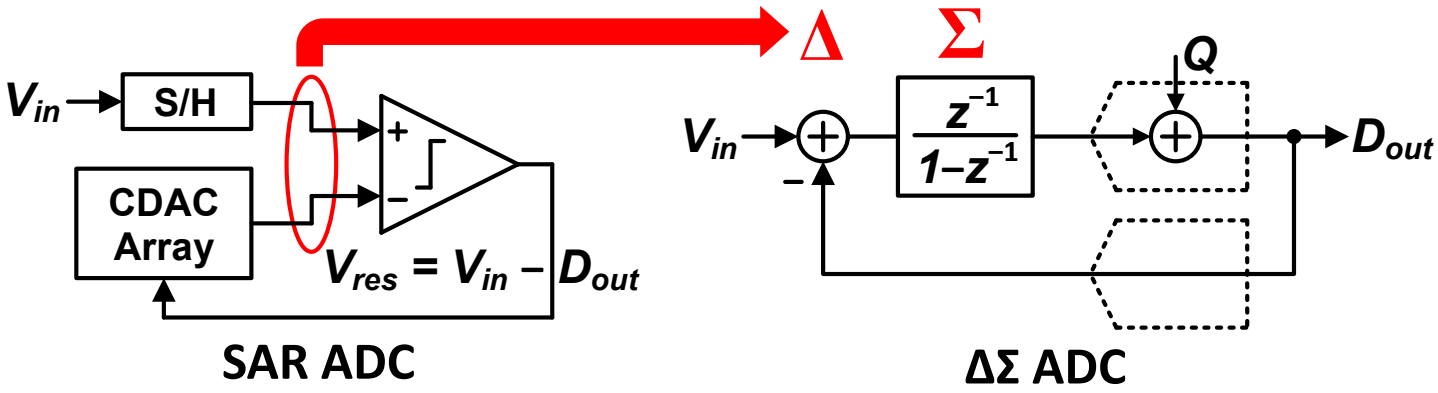
- Motivation
- Review of Prior Work
- Proposed TI NS SAR ADC
- Measurement Results
- Conclusions

Motivation

- SAR ADC
  - Advantages: simple, mostly digital, scaling friendly, power efficient ☺
  - Disadvantages: difficult to achieve high resolution ☹
- ΔΣ ADC
  - Advantages: high resolution, simple quantizer ☺
  - Disadvantages: require OTA, power hungry, scaling unfriendly ☹

Motivation

- Noise-Shaping (NS) SAR ADC
  - A hybrid of SAR and ΔΣ ADC
  - Advantages: high resolution, high energy efficiency ☺
  - Disadvantages: slow quantizer, limited bandwidth ☹



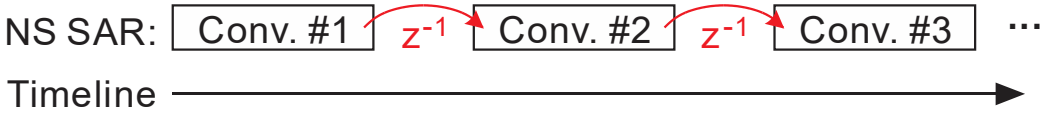
Motivation

- Time-Interleaved (TI) NS SAR ADC
  - Advantages:
  - ✓ Wideband applications ☺
  - ✓ Higher energy efficiency (than pipelined or CT ΔΣ ADCs) ☺
  - ✓ Insensitive to channel mismatch ☺
  - Disadvantages: TI for NS SAR is non-trivial ☹

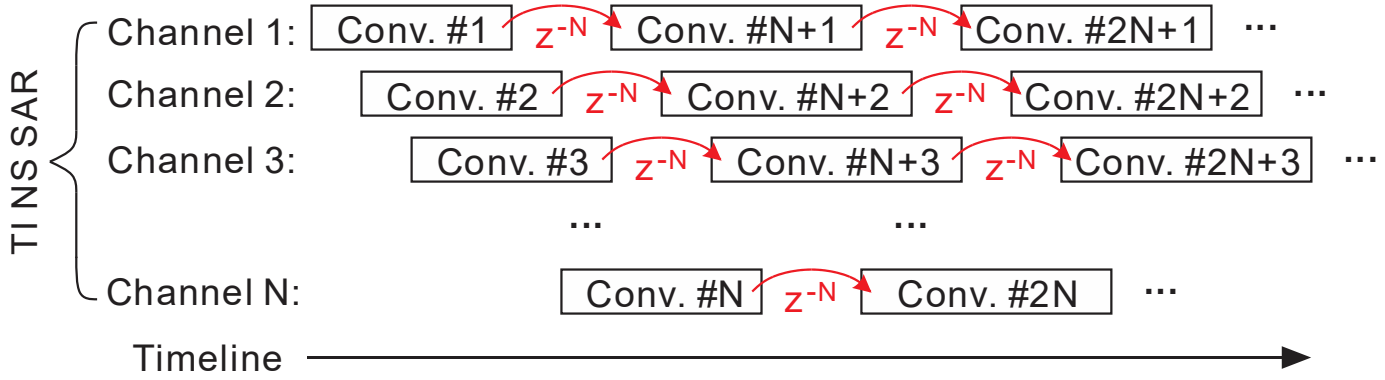
TI for NS SAR is Non-Trivial

- Dependency on quantization error memory

① Single-channel NS SAR ADC: $NTF = 1 - z^{-1}$

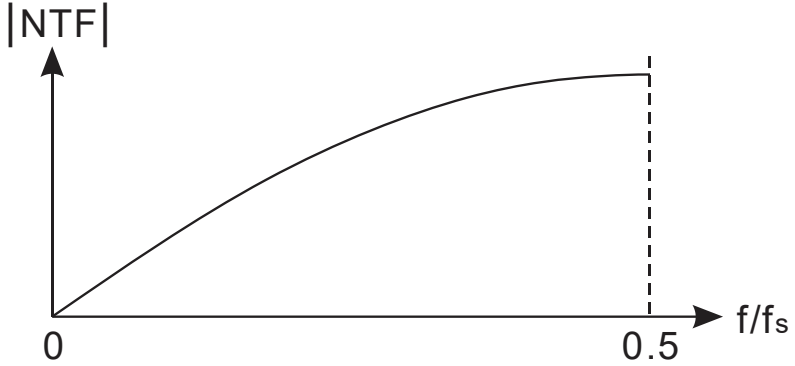


② TI NS SAR ADC: $NTF = 1 - z^{-N}$

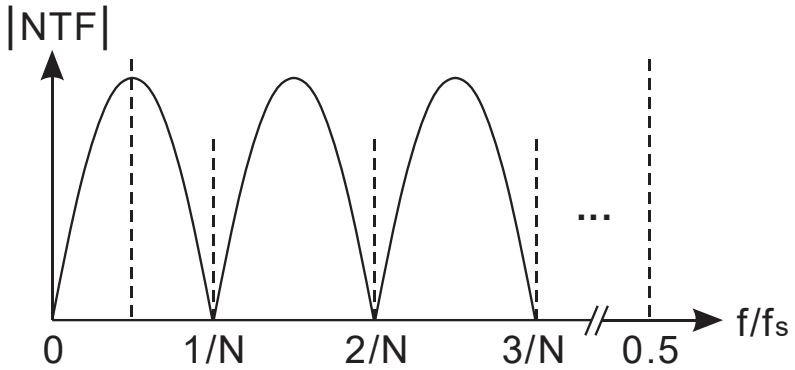


TI for NS SAR is Non-Trivial

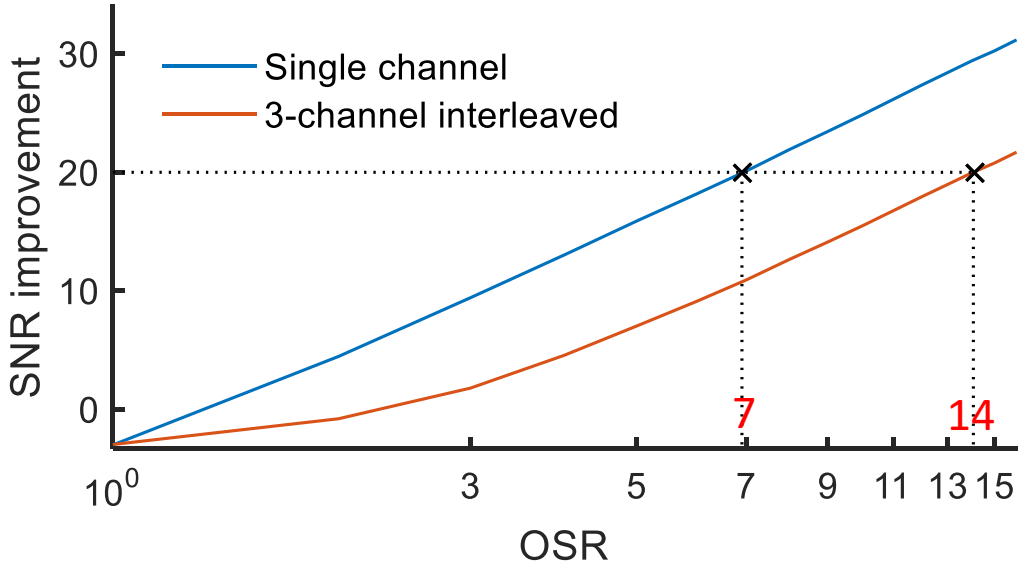
$NTF = 1 - z^{-1}$
(Single-channel NS SAR ADC)



$NTF = 1 - z^{-N}$
(TI NS SAR ADC)



TI for NS SAR is Non-Trivial



- To achieve the same SNR, much higher OSR is required.
- Inefficient noise shaping effect.

Outline

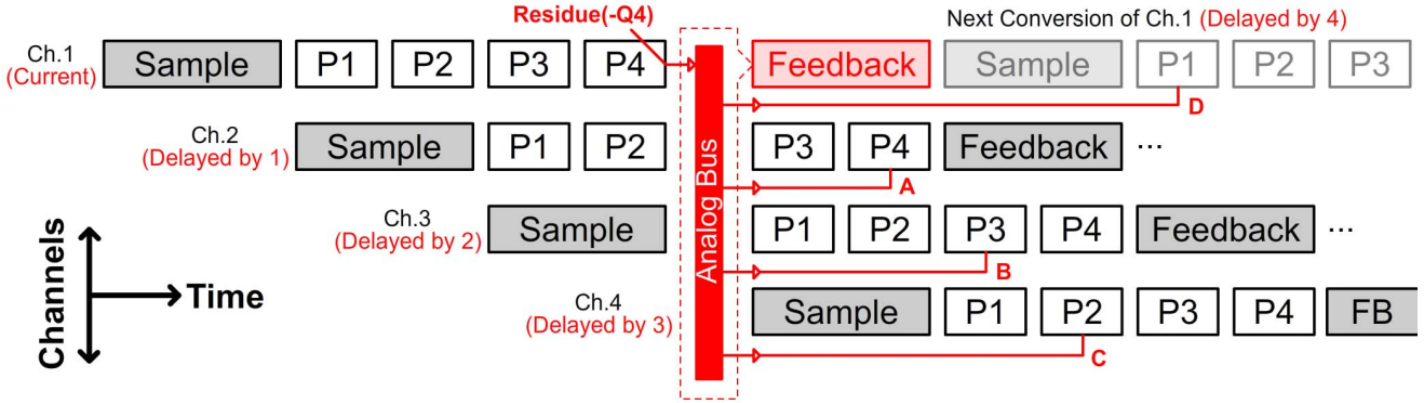
- Motivation
- Review of Prior Work
- Proposed TI NS SAR ADC
- Measurement Results
- Conclusions

Prior TI NS SAR Work

- Prior TI NS SAR [L. Jie *ISSCC 2019*]

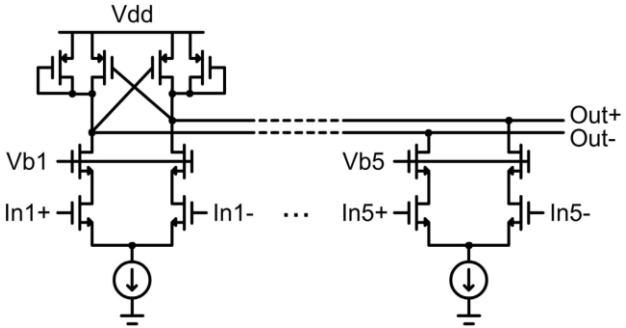
  Share quantization error memory in all the channels ☺

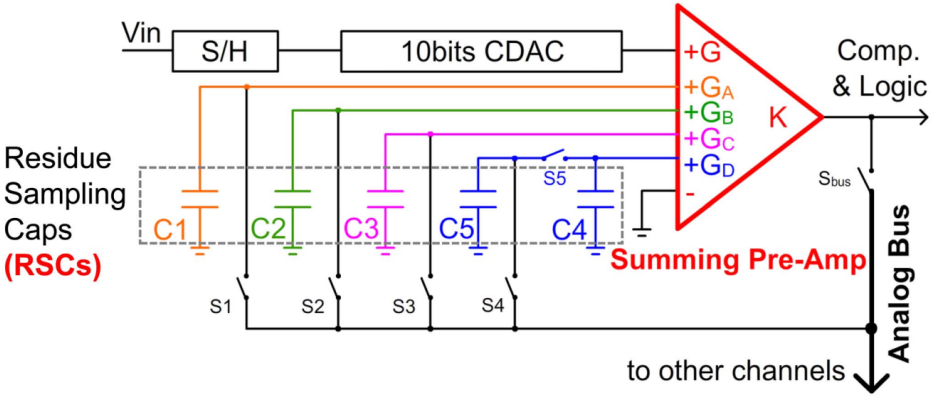
  Similar to single-channel NS SAR ☺



$$NTF(z) = (1 - 0.5z^{-1})^4$$

Prior TI NS SAR Work





- EF-based architecture ☹
- Static amplifier (power hungry, always active) ☹
  (accounts for 45% of the total power) ☹
- Amplifier gain is PVT-sensitive ☹
- NTF zeros at 0.5 (far away from 1) ☹

Outline

- Motivation
- Review of Prior Work
- Proposed TI NS SAR ADC
- Measurement Results
- Conclusions

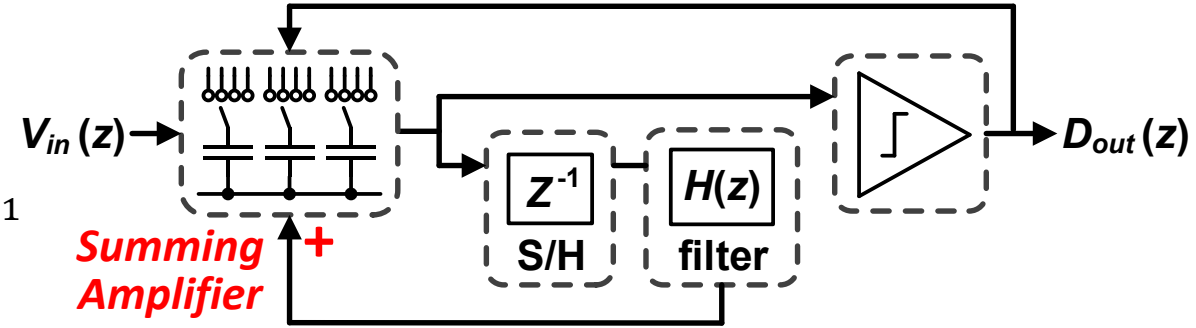
Proposed TI NS SAR with CIFF-based Architecture

- CIFF: Cascade of Integrators with Feed-Forward
  - ✓ Simple, fully-dynamic, low-power, wide-band ☺
  - ✓ No static amplifiers ☺
  - ✓ Only dynamic comparators ☺
  - ✓ Low-duty-cycle summing comparator ☺
  - ✓ NTF set by device ratios, highly robust ☺
  - ✓ NTF zeros at 0.75 (closer to 1) ☺
  - ✓ Low-duty-cycle sensor applications ☺

Proposed TI NS SAR with CIFF-based Architecture

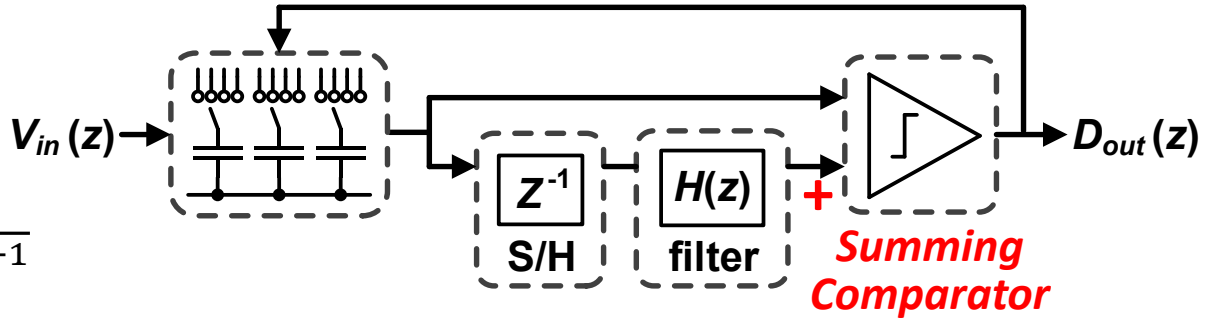
EF-based Architecture:

$$NTF(z) = 1 - H(z)z^{-1}$$

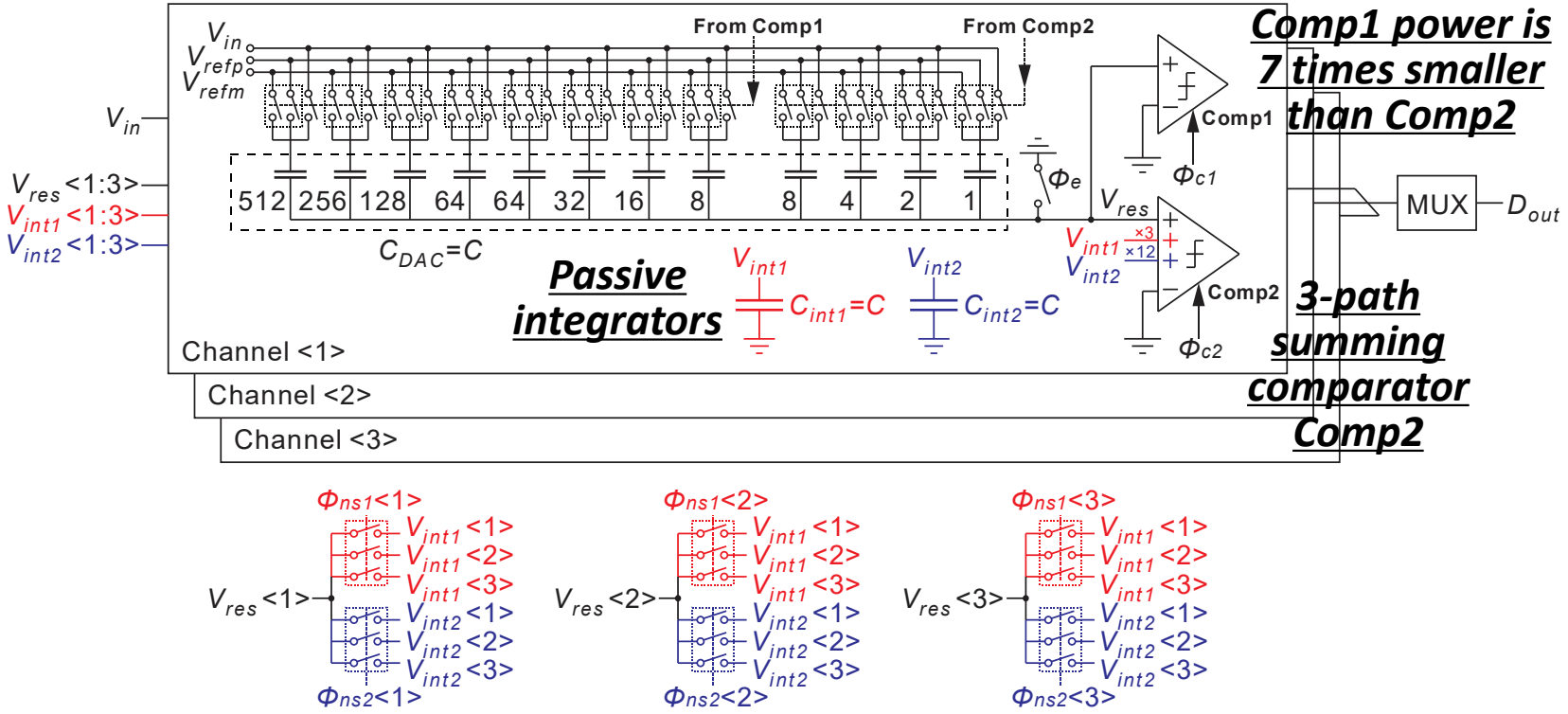


CIFF-based Architecture:

$$NTF(z) = \frac{1}{1 + H(z)z^{-1}}$$

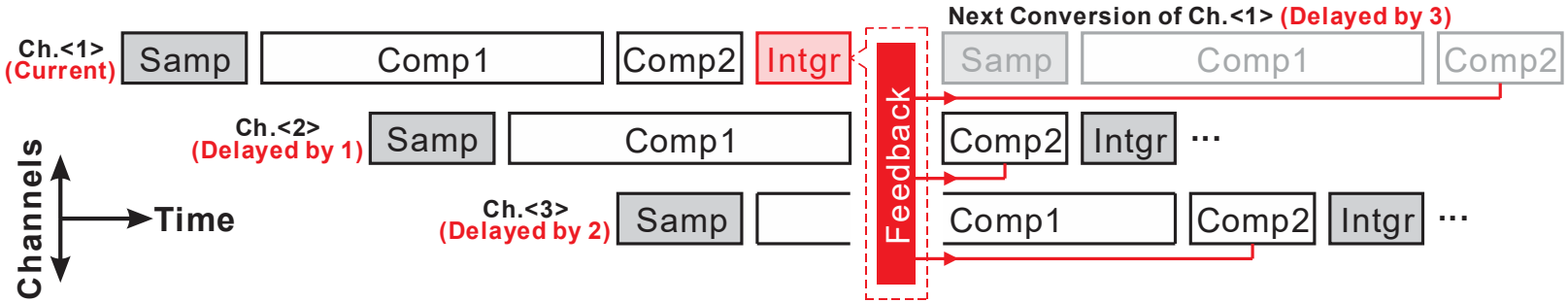


Proposed TI NS SAR with CIFF-based Architecture



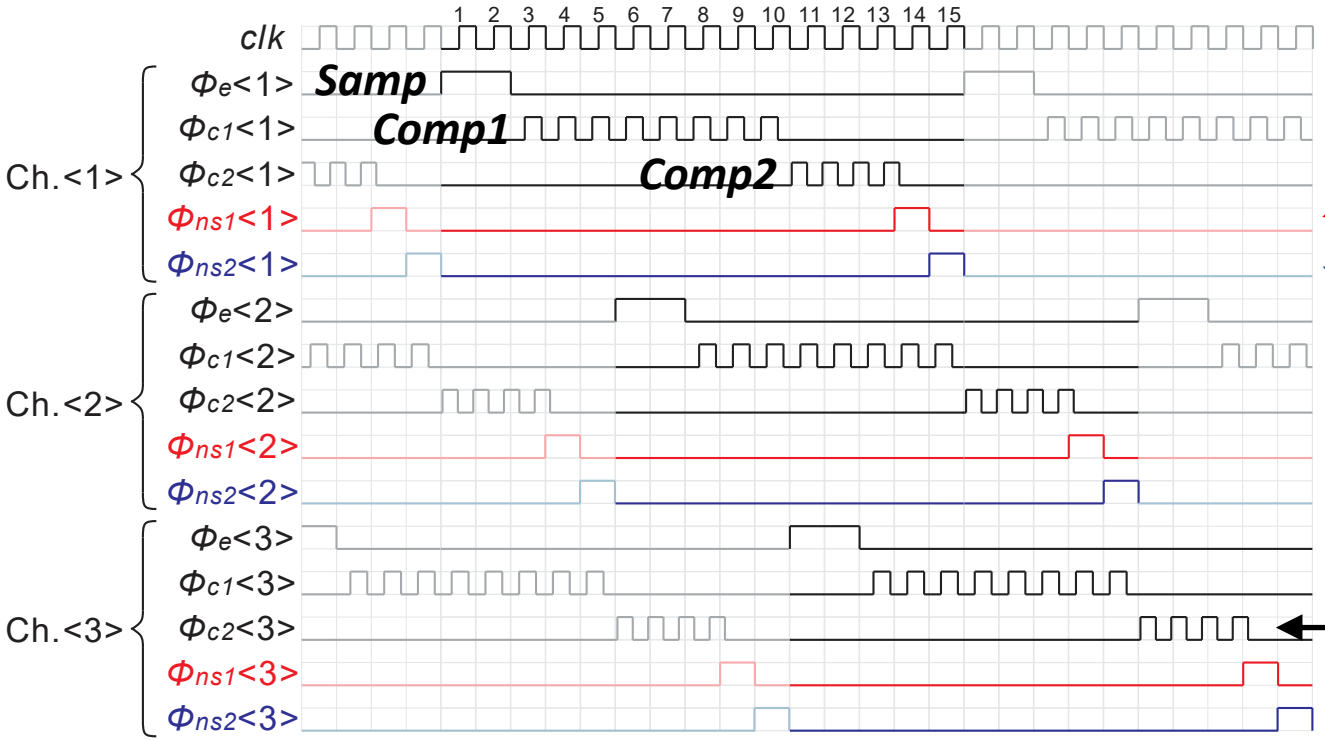
Proposed TI NS SAR with CIFF-based Architecture

- Way of Interleaving
  - ✓ Share the integrated residuals V_{int1} and V_{int2} in all the channels
  - ✓ Comp2 sums the integrated residuals with the CDAC residual V_{res}.



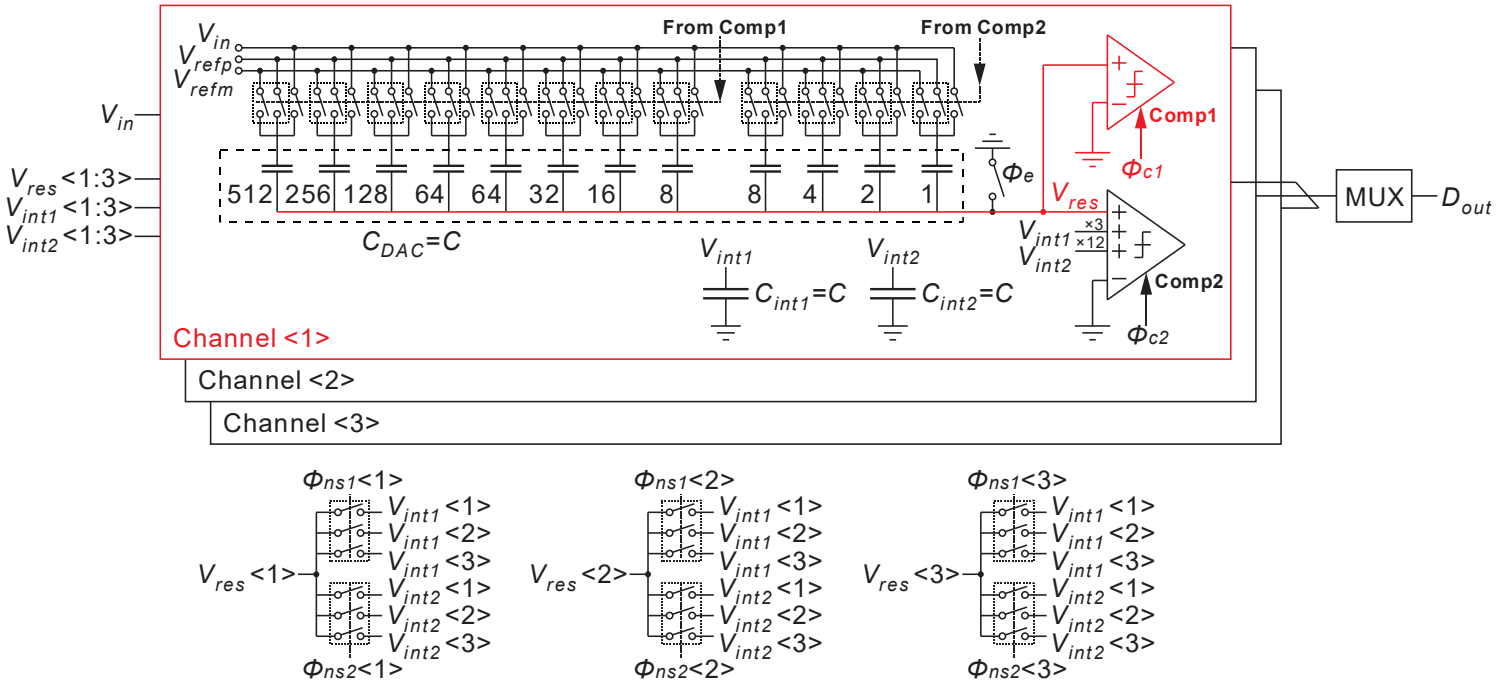
The comparator power consumption is 2.2 times smaller than the static amplifier + comparator power consumption of [L. Jie *ISSCC 2019*].

Proposed TI NS SAR with CIFF-based Architecture



Step 1 in Channel <1>

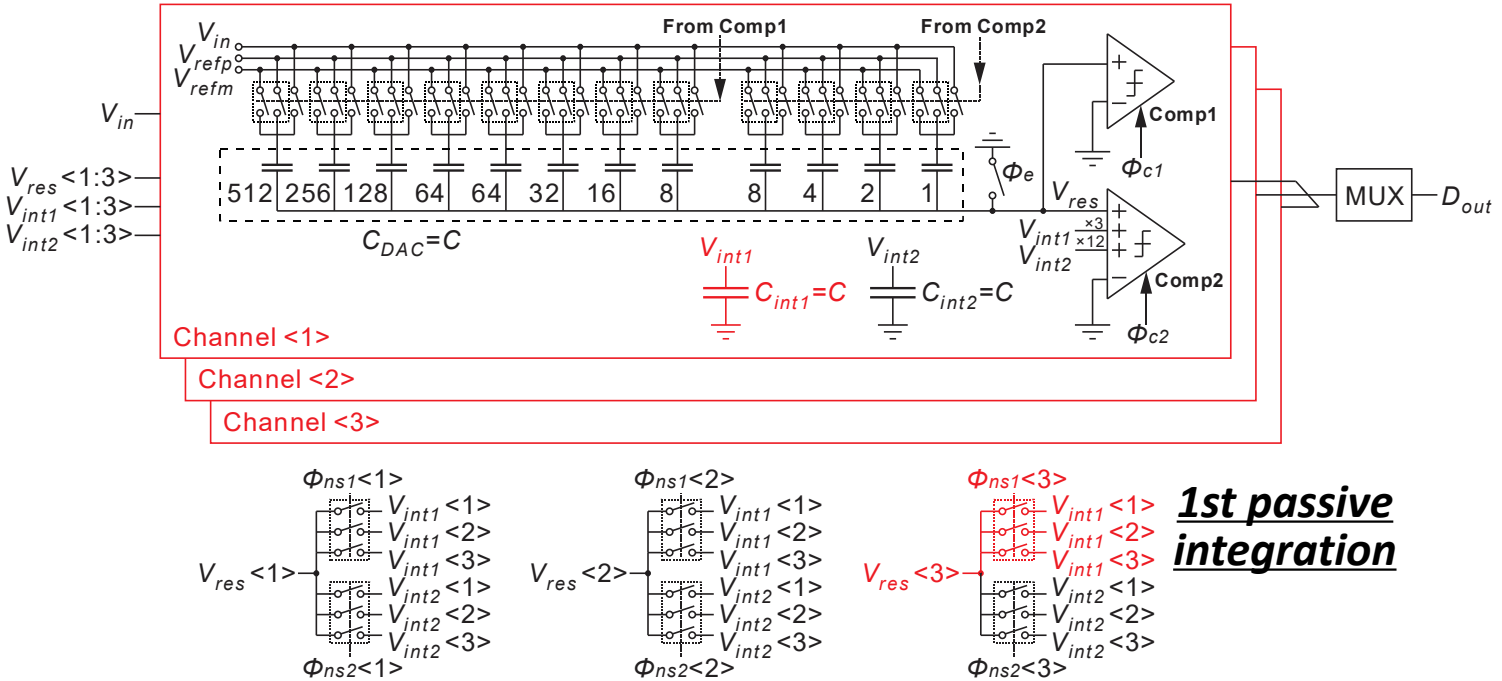
Comp1 determines the first 8 bits
(10-bit CDAC with 2 redundant bits)



Step 2 in Channel <1>

$$V_{int1}(z) = \frac{0.25z^{-1}}{1 - 0.75z^{-1}} V_{res}(z)$$

The C_{DAC} of previous channel shares charges with C_{int1} of all the three channels. (C_{int1} of all the three channels are connected.)

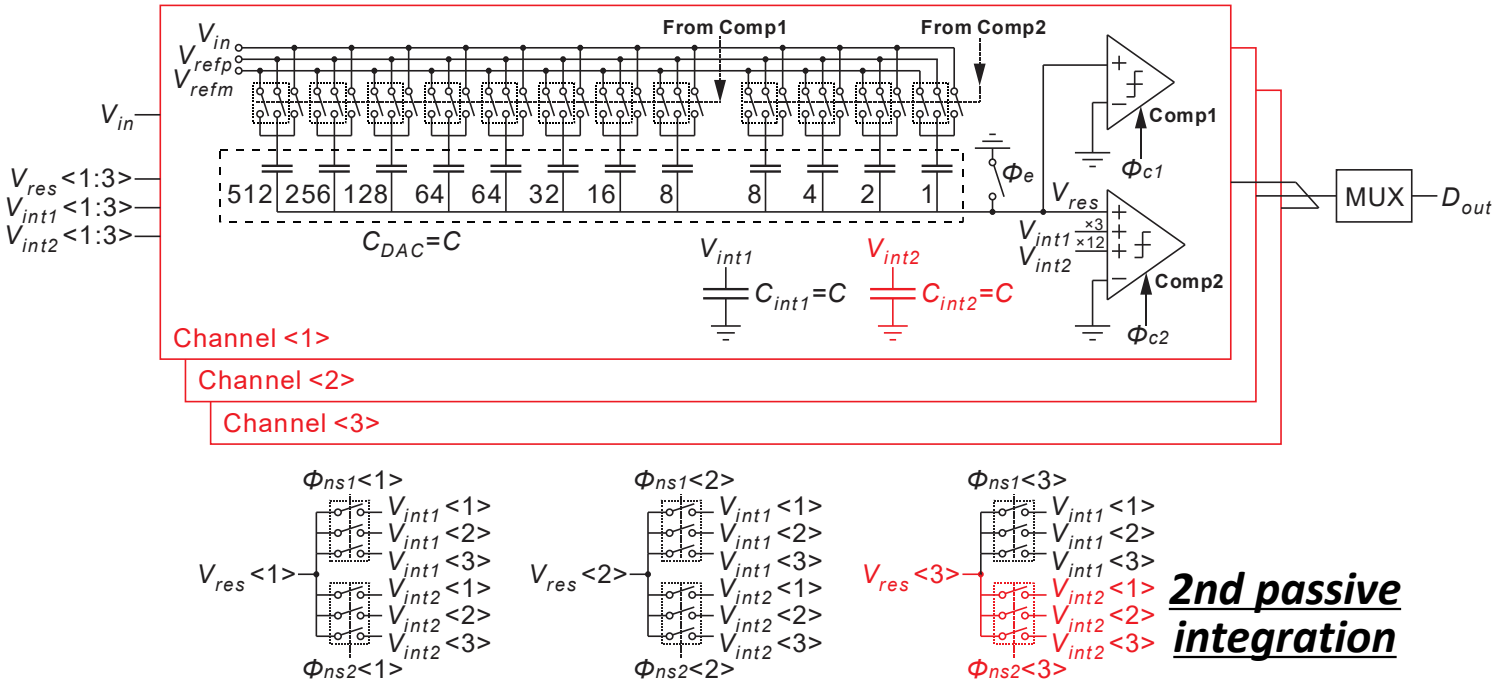


1st passive integration

Step 3 in Channel <1>

$$V_{int2}(z) = \frac{0.25}{1-0.75z^{-1}} V_{int1}(z) = \frac{0.25^2 z^{-1}}{(1-0.75z^{-1})^2} V_{res}(z)$$

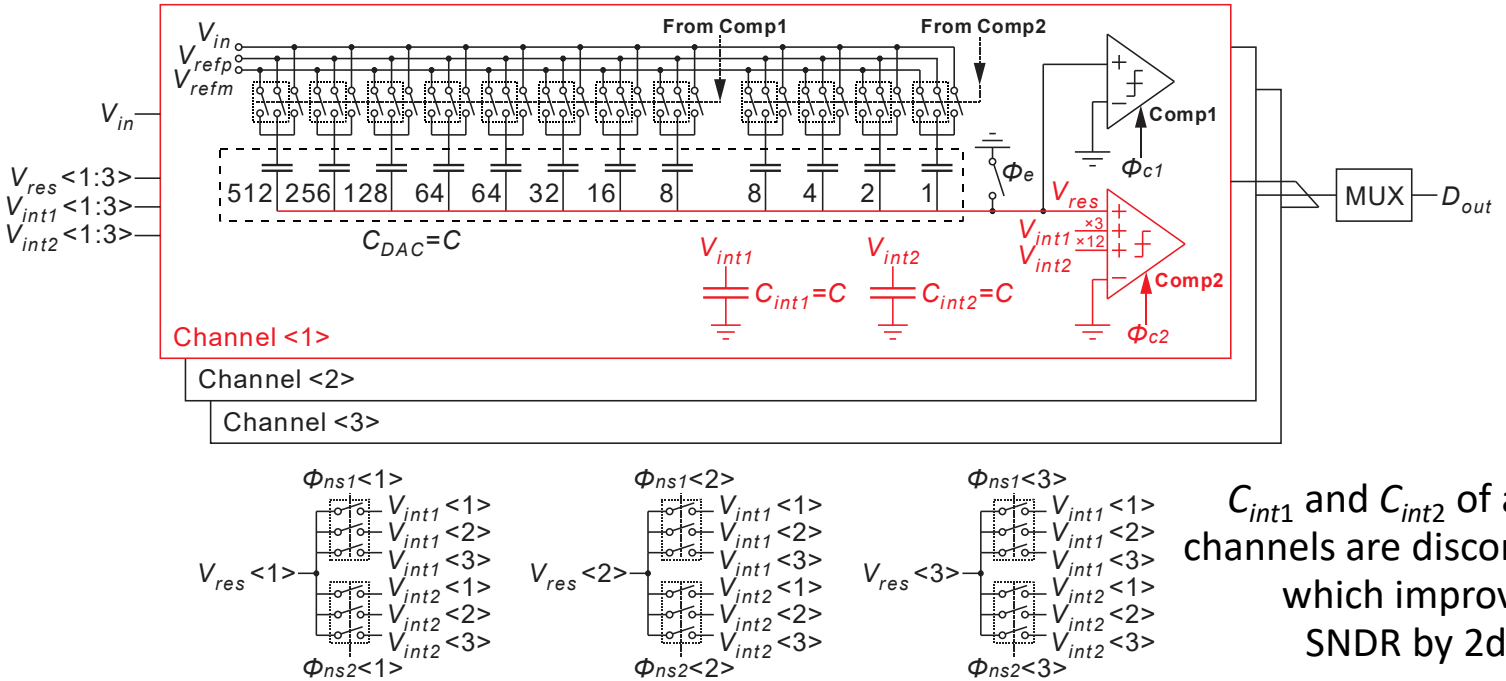
The C_{DAC} of previous channel shares charges with C_{int2} of all the three channels. (C_{int2} of all the three channels are connected.)



Step 4 in Channel <1>

Comp2 determines the last 4 bits.

Channel isolation reduces the interference between channels.

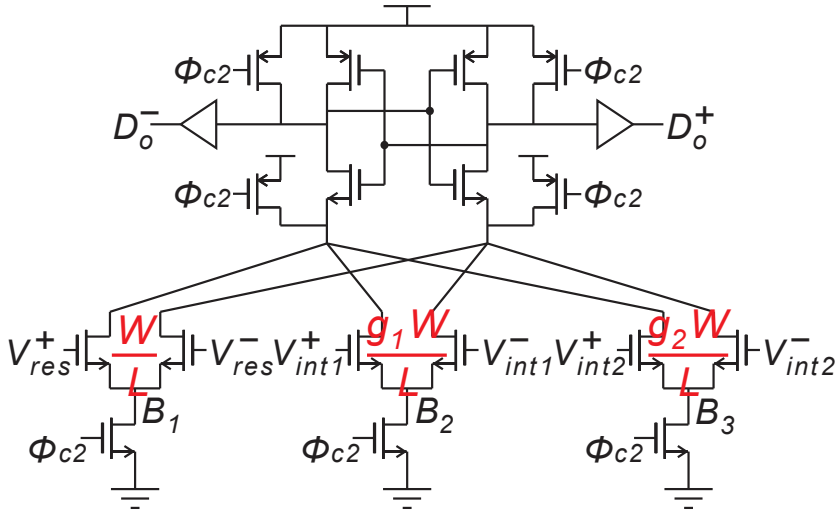


C_{int1} and C_{int2} of all the channels are disconnected, which improves SNDR by 2dB

Step 4 in Channel <1>

$$V_{int1}(z) = \frac{0.25z^{-1}}{1 - 0.75z^{-1}} V_{res}(z)$$

$$V_{int2}(z) = \frac{0.25^2 z^{-1}}{(1 - 0.75z^{-1})^2} V_{res}(z)$$



$$V_{res} + g_1 V_{int1} + g_2 V_{int2}$$

- Gain Loss Exists

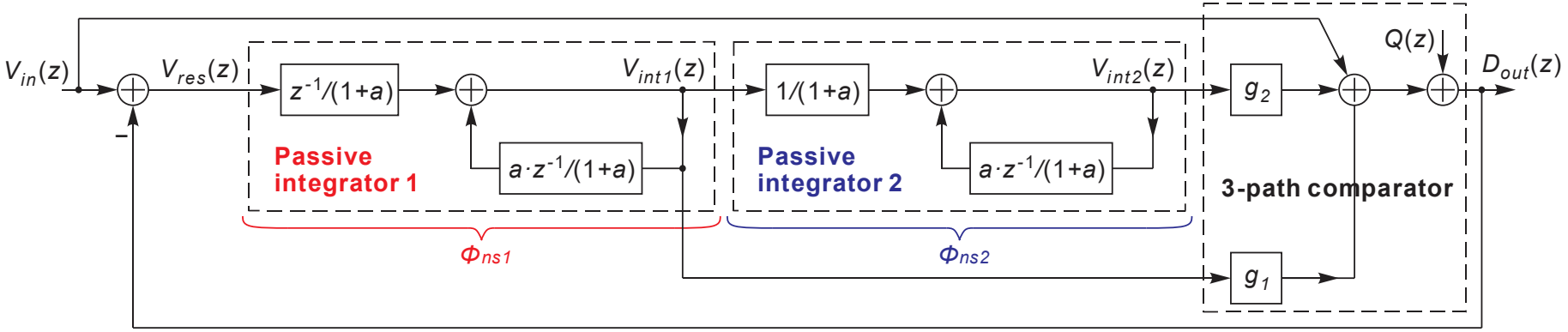
✓ Comparator result is a 1-bit sign.

✓ What is needed here is a relative gain between V_{res} and V_{int1}, V_{int2}.

✓ Can be easily implemented by sizing the comparator input transistors.

Signal Flow Diagram

Assume $C_{int1} = aC_{DAC}/3, C_{int2} = aC_{DAC}/3$



$$D_{out}(z) = V_{in}(z) + \frac{\left(1 - \frac{a}{1+a}z^{-1}\right)^2}{1 + \frac{(1+a)g_1 + g_2 - 2a(1+a)}{(1+a)^2}z^{-1} + \frac{-ag_1 + a^2}{(1+a)^2}z^{-2}} Q(z)$$

$$g_1 = a, g_2 = a(1+a) \Longrightarrow D_{out}(z) = V_{in}(z) + \left(1 - \frac{a}{1+a}z^{-1}\right)^2 Q(z)$$

$$g_1 = 3, g_2 = 12 \Longrightarrow D_{out}(z) = V_{in}(z) + (1 - 0.75z^{-1})^2 Q(z)$$

Accuracy of Noise Transfer Function

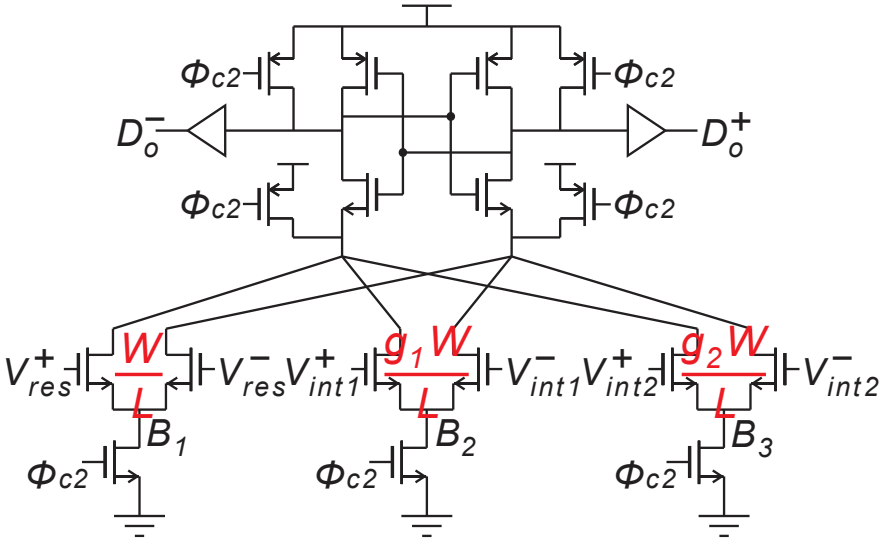
$$D_{out}(z) = V_{in}(z) + \frac{\left(1 - \frac{a}{1+a}z^{-1}\right)^2}{1 + \frac{(1+a)g_1 + g_2 - 2a(1+a)}{(1+a)^2}z^{-1} + \frac{-ag_1 + a^2}{(1+a)^2}z^{-2}} Q(z)$$

- Zero locations: $a/(1+a)$
  - Determined by capacitor ratio C_{int}/C_{DAC}
  - PVT insensitive
- Pole locations related to:
  - a (PVT insensitive)
  - g_1 and g_2 (PVT insensitive?)

Accuracy of g_1 and g_2

V_{th} mismatch of input transistor:

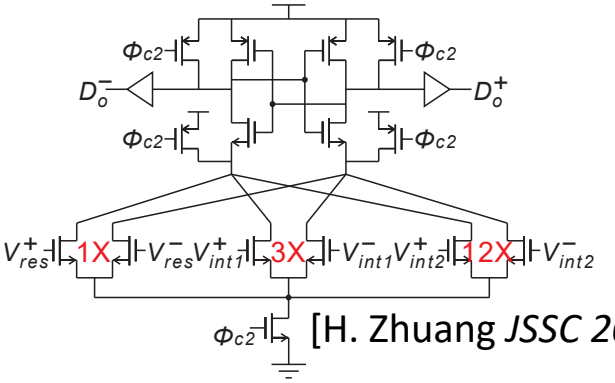
- Without mismatch
  - g_1 and g_2 are robust against PVT
- With differential-mode mismatch, i.e. $V_{th\_left} \neq V_{th\_right}$
  - Only result in comparator offset
  - Do not affect g_1 and g_2
- With common-mode mismatch, i.e. $(V_{th\_left} + V_{th\_right})/2$ varies
  - Affect g_1 and g_2



$$V_{res} + g_1 V_{int1} + g_2 V_{int2}$$

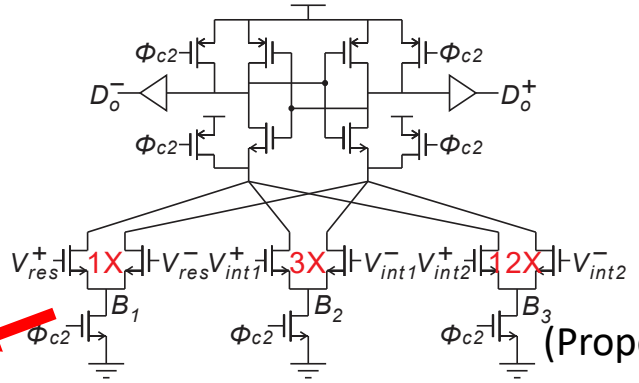
Accuracy of g_1 and g_2

Source of input pairs connected:



[H. Zhuang *JSSC 2019*]

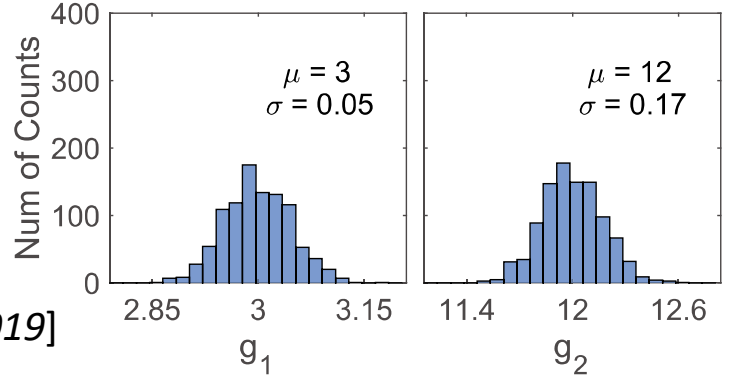
Source of input pairs separated:

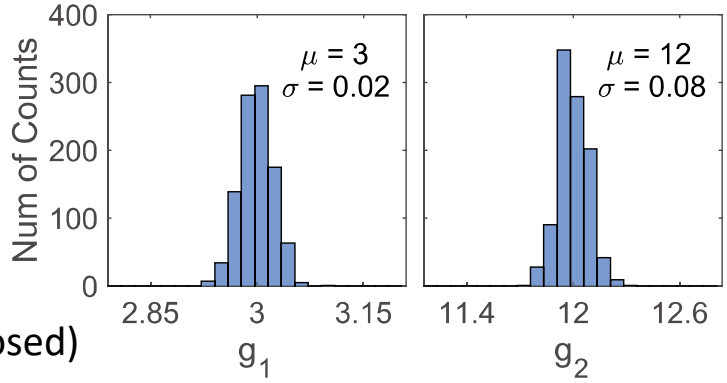


(Proposed)

(degenerate common-mode mismatch)

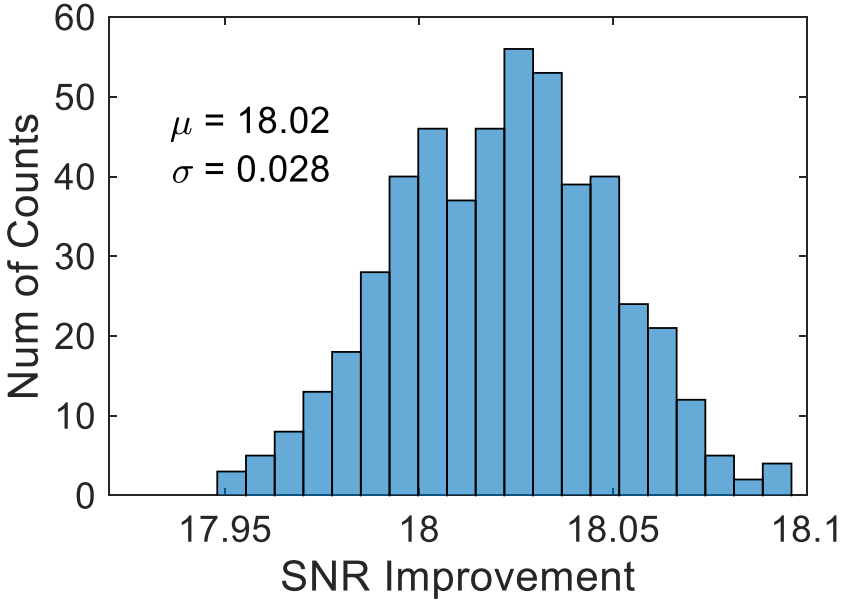
Monte-Carlo Simulation with 1000 cases:





Effect of g_1 and g_2 Variations

SNR improvement from NS: (source of input pairs separated)



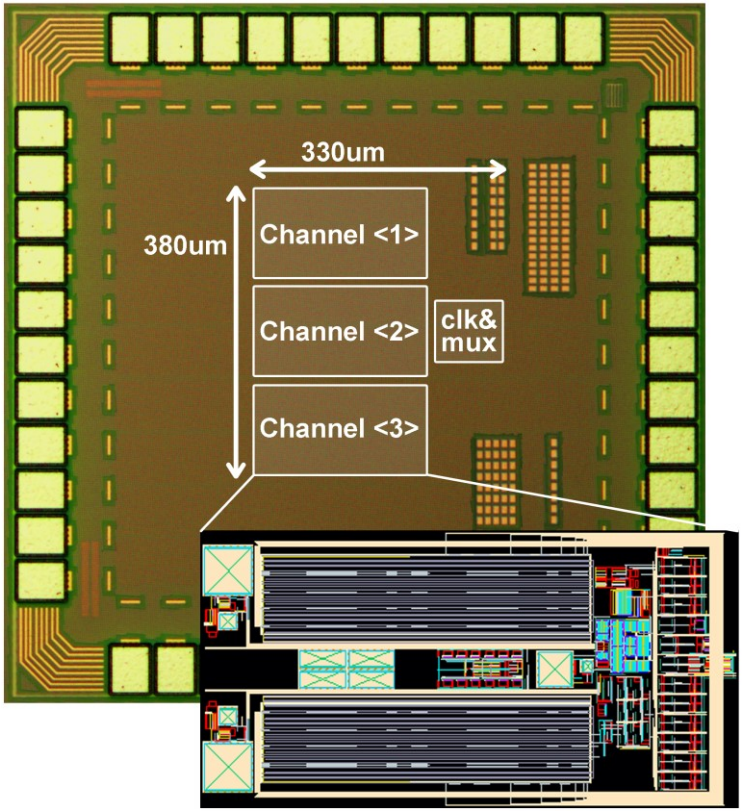
- With the source of input pairs separated, we have $|\Delta\mathrm{SNR}| < 0.1\mathrm{dB}$.
- The proposed TI NS SAR ADC is highly robust.

Outline

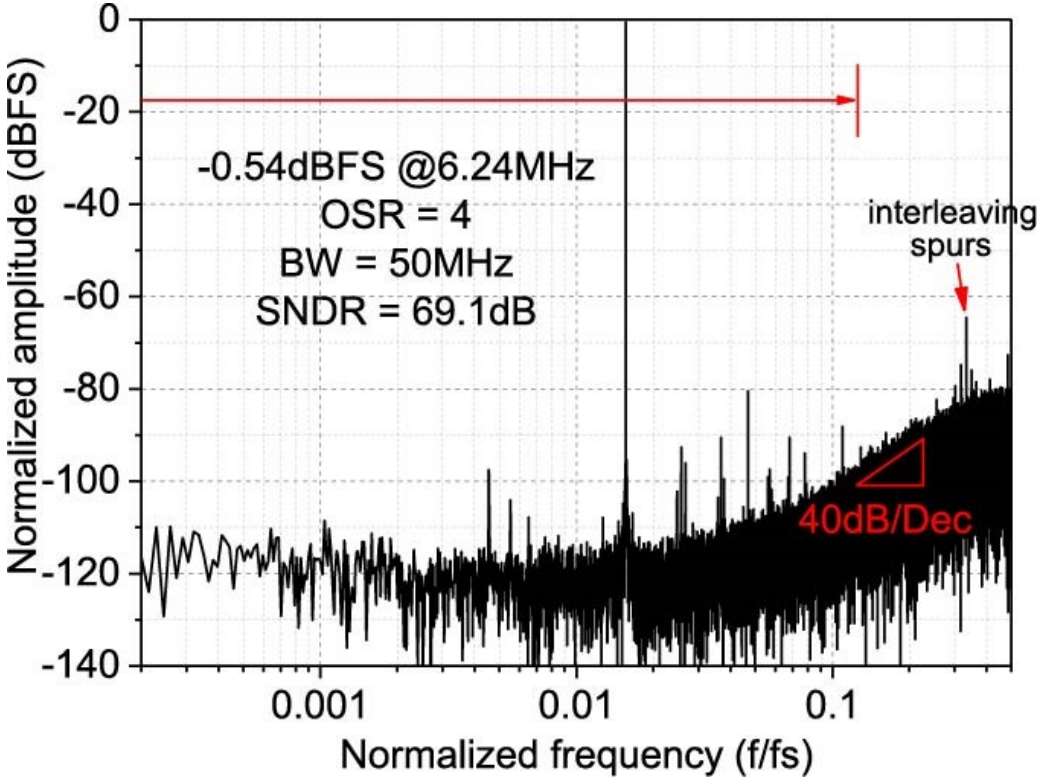
- Motivation
- Review of Prior Work
- Proposed TI NS SAR ADC
- Measurement Results
- Conclusions

Measurement Results

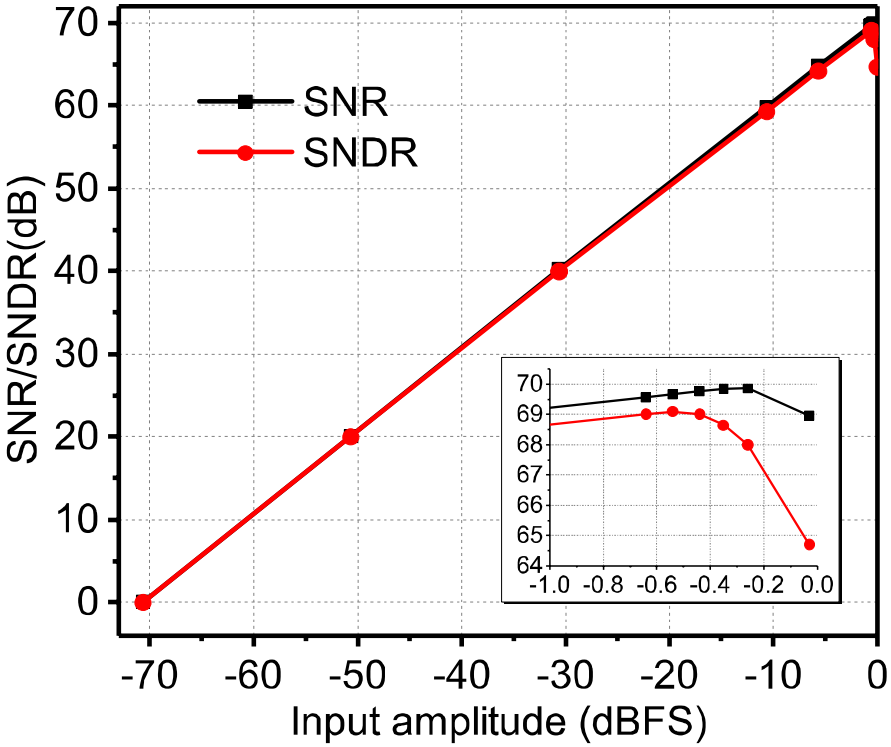
- 40nm CMOS process
- 380μm×330μm
- Sampling rate: 400MS/s
- Supply: 1.1V
- Power consumption: 8.5mW

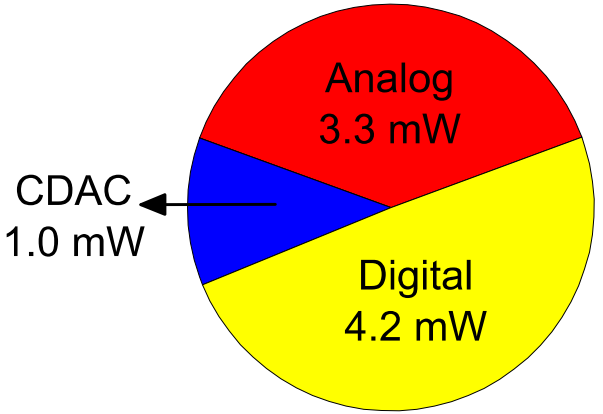


Measured Output Spectrum



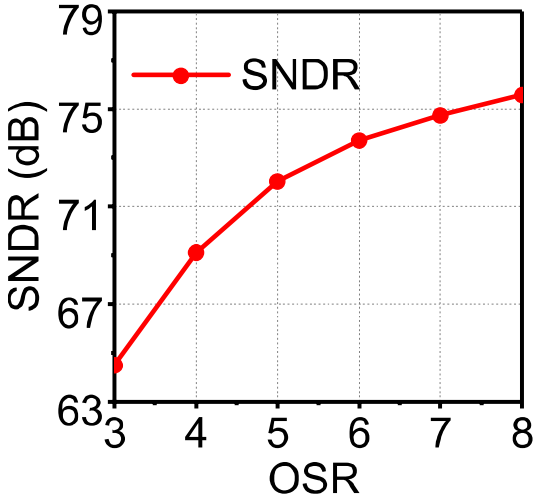
Measured SNR/SNDR and Power

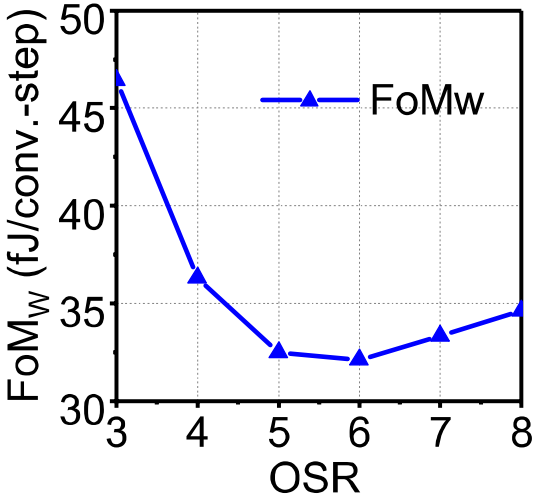




Total = 8.5 mW

Measured SNDR and FoM vs. OSR





- The best FoM$_W$ is at OSR of 6, where FoM$_W$ is 32.1 fJ/conv.-step and SNDR is 73.7 dB.

Performance Comparisons

	This work		[7]	[8]	[9]
Architecture	**TI NS SAR (CIFF-based)**		TI NS SAR (EF-based)	CT ΔΣ	CT ΔΣ
Fully-Dynamic	**Yes**		No	No	No
NTF Set by Device Ratio	**Yes**		No	No	No
Technology (nm)	**40**		40	65	28
Area (mm^2)	**0.125**		0.061	0.07	0.25
Supply Voltage (V)	**1.1**		1	1.4	1.2/1.5
Power (mW)	**8.5**		13	13.3	64.3
Sampling Rate (MS/s)	**400**		400	6000	2000
OSR	**4**	**6**	4	50	20
Bandwidth (MHz)	**50**	**33.3**	50	60	50
SNDR (dB)	**69.1**	**73.7**	70.4	67.6	79.8
FoM_W (fJ/conv.-step)	**36.3**	**32.1**	48.1	56.5	80.5

Conclusions

- A novel TI NS SAR based on the CIFF architecture
- Simple, fully-dynamic, low-power, and wide-band
- Static amplifiers are replaced by dynamic comparators, saving energy
- Dynamic summing comparator is only active 1/5 of the time, further saving energy
- It eliminates the dependence of NTF on the amplifier gain that is PVT sensitive
- Its NTF is set by device ratios and highly robust against PVT variations
- NTF zeros at 0.75 are closer to 1 with better NS effect
- Well suited for low-duty-cycle sensor applications

References

- [1] **Haoyu Zhuang**, et al., “A Fully Dynamic Low-Power Wideband Time-Interleaved Noise-Shaping SAR ADC,” ***IEEE Journal of Solid-State Circuits***, vol. 56, no. 9, pp. 2680-2690, April 2021.
- [2] **Haoyu Zhuang**, et al., “A Second-Order Noise-Shaping SAR ADC With Passive Integrator and Tri-Level Voting,” ***IEEE Journal of Solid-State Circuits***, vol. 54, no. 6, pp. 1636-1647, March 2019.


thank
you!