A 13-Bit ENOB Third-Order Noise-Shaping SAR ADC Employing Hybrid Error Control Structure and LMS-Based Foreground Digital Calibration

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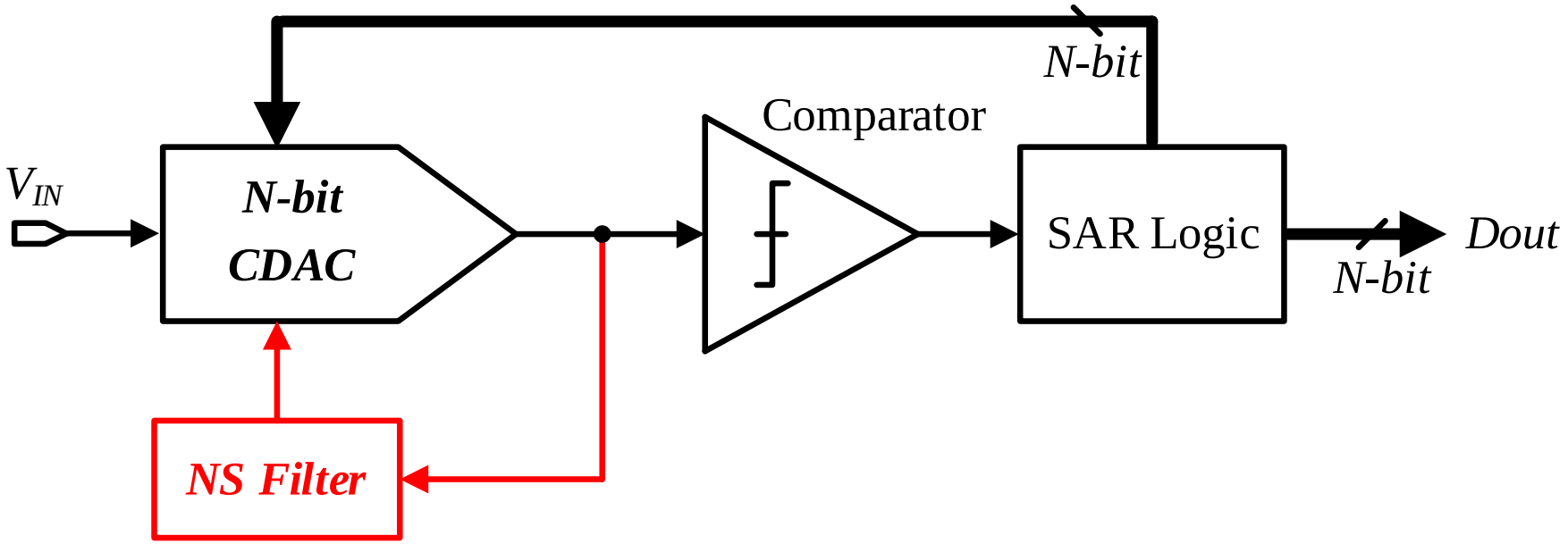
MICS

Outline

- Background
- Proposed Hybrid Noise-Shaping SAR ADC
- Foreground Capacitor Mismatch Calibration
- Measurement Results
- Conclusion

Background

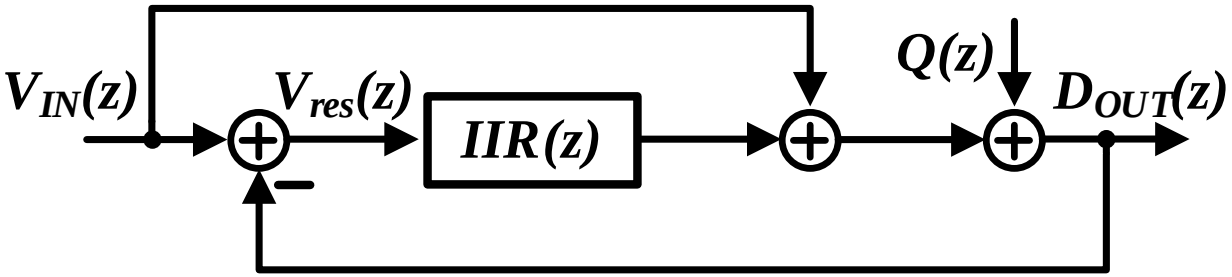


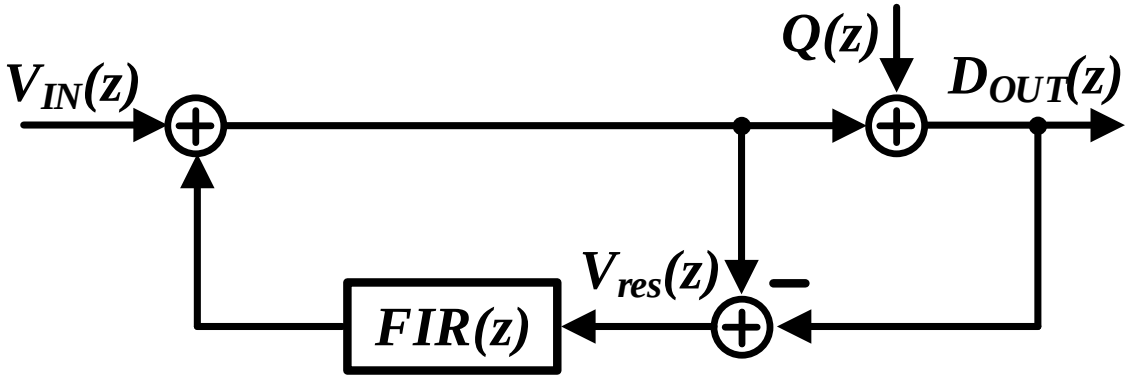
- ✓ Pros of NS SAR ADC
  - SAR ADC: Low Power
  - Sigma-Delta ADC: High Resolution
- ✓ Process of Quantization
  - Conversion →V_{res} Filtering→Signal Summation

- ✓ Low OSR(<10), High SNR(>80 dB)

NS Filter Order >3

Background





◆CIFF：

- Integrator Composed IIR Filter
- Summed With Input Signal At The Input of Comparator
- NTF=1/(1+IIR(z))

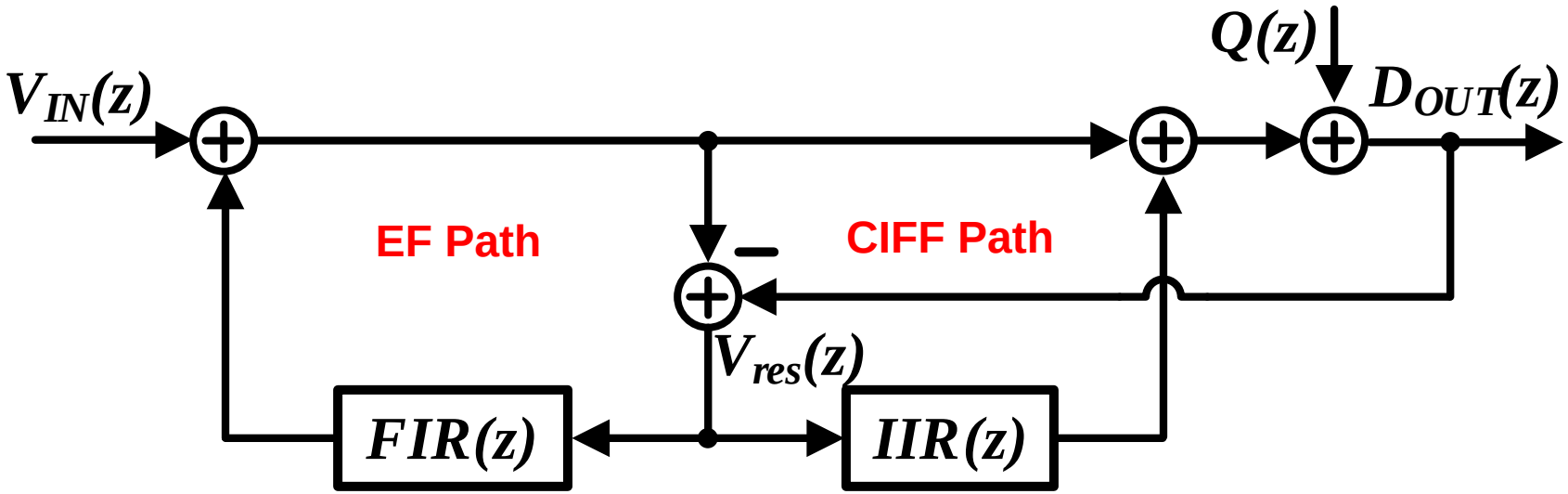
✓ Stable and Robust
× More Active/Passive Integrator
× Power Hungry and Complex

◆EF:

- SC-Based FIR
- Summed with The Next Input Signal Directly
- NTF=1-FIR(z)

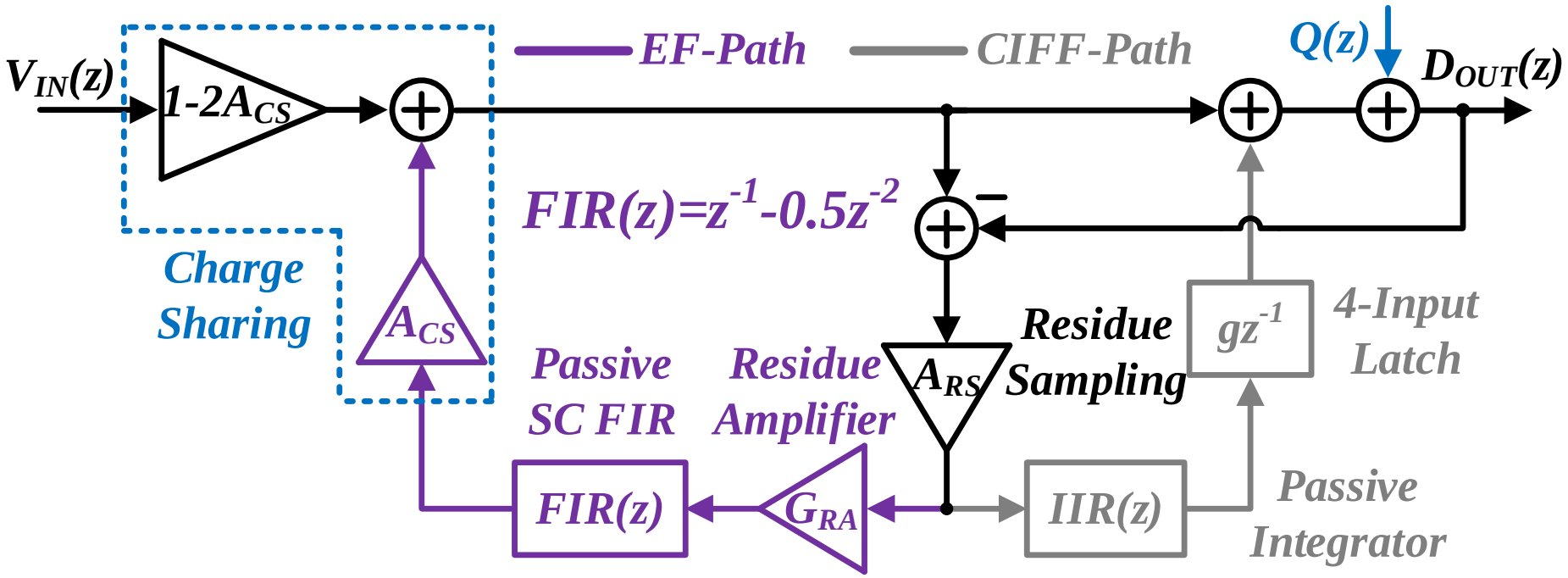
✓ Simple With Delay Cell
× Accurate Gain of Residue Amplifier
× Sensitive to PVT

Proposed Hybrid Noise-Shaping SAR ADC



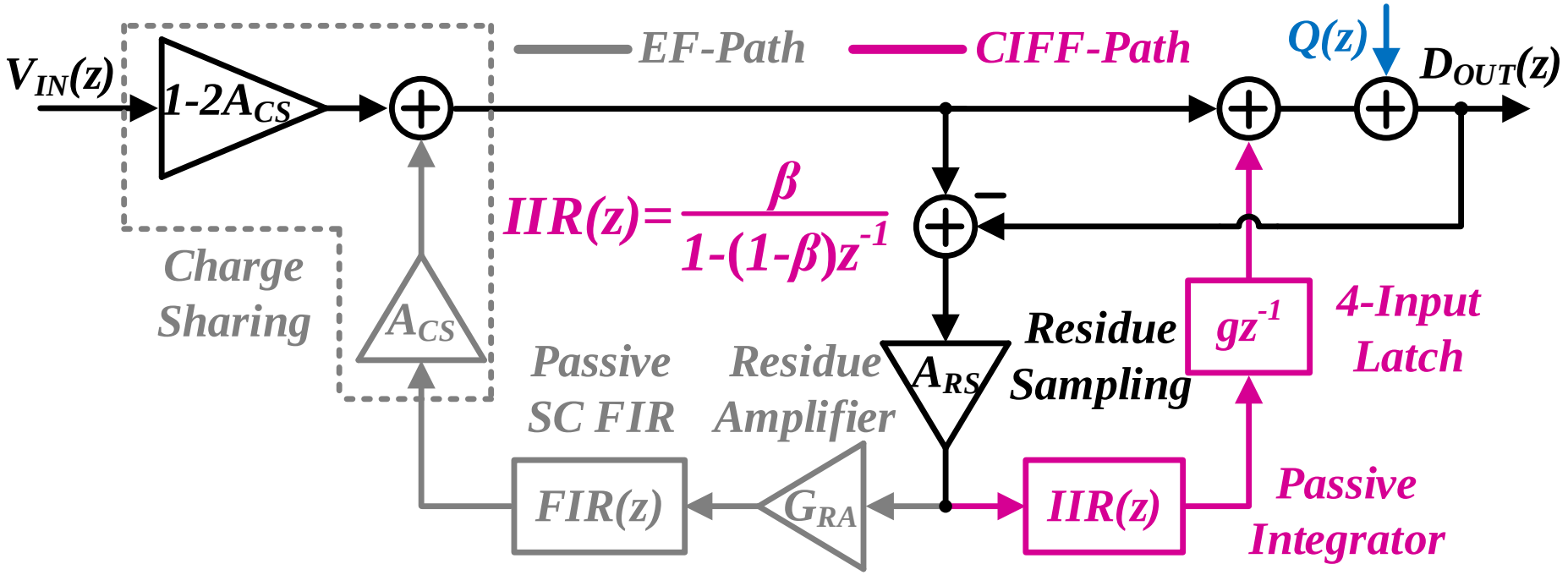
- ✓ Combined NTF: $NTF_{HEC} = \dfrac{1 - FIR(z)}{1 + IIR(z)}$
- ✓ Realized EF And CIFF Together
- ✓ For a Third-Order NS SAR ADC, Filter Order <2 and Simplify The Design
- ✓ More Stable Than Conventional Third-Order IIR/FIR

Proposed Hybrid Noise-Shaping SAR ADC



- ✓ EF Path: Residue Sample (A_{RS}), Residue Amplify (G_{RA}) and SC-Based FIR(A_{CS})
- ✓ EF Path Gain $K_{EF}= A_{RS}G_{RA}A_{CS}$
- ✓ NTF of EF Path: $NTF_{EF} = 1 - K_{EF}\left(z^{-1} - 0.5z^{-2}\right)$

Proposed Hybrid Noise-Shaping SAR ADC



- ✓ CIFF Path: Passive Integrator and 4-input Comparator
- ✓ Gain Ratio of Signal Path and Integration Path: 1/g, $C_{int}=\frac{1-\beta}{\beta}C_{DAC}$
- ✓ CIFF Path NTF: $NTF_{CIFF}=\frac{1}{1+A_{RS}gz^{-1}IIR(z)}$

Proposed Hybrid Noise-Shaping SAR ADC

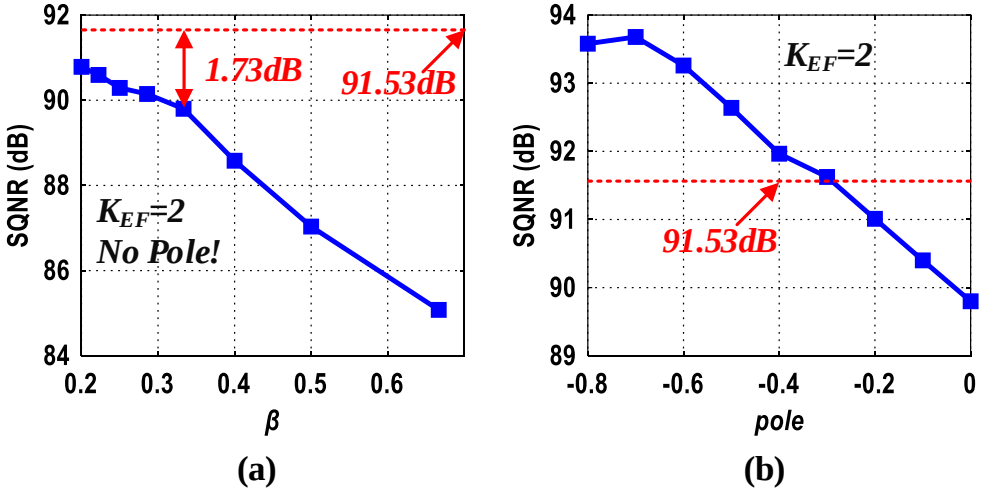
EF+CIFF Noise Transfer Function：

$$NTF=\frac{1-K_{EF}\times FIR(z)}{1+gA_{RS}z^{-1}\times IIR(z)}=\frac{(1-K_{EF}\times(z^{-1}-0.5z^{-2}))\times(1-(1-\beta)z^{-1})}{1-((1-\beta)-\beta gA_{RS})z^{-1}}$$

- ✓ One Pole，Three Zeros
- ✓ Noise Shaping Capability is Dependent With The Positions of Pole and Zeros
- ✓ Need to Optimize The Parameters of β, g, A_{RS}, K_{EF} For The Optimal Dynamic Performance, Area and Power

Proposed Hybrid Noise-Shaping SAR ADC

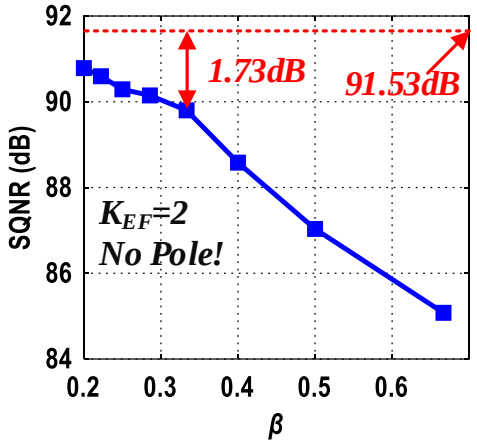
$$NTF=\frac{1-K_{EF}\times FIR(z)}{1+gA_{RS}z^{-1}\times IIR(z)}=\frac{(1-K_{EF}\times(z^{-1}-0.5z^{-2}))\times(1-(1-\beta)z^{-1})}{1-((1-\beta)-\beta gA_{RS})z^{-1}}$$



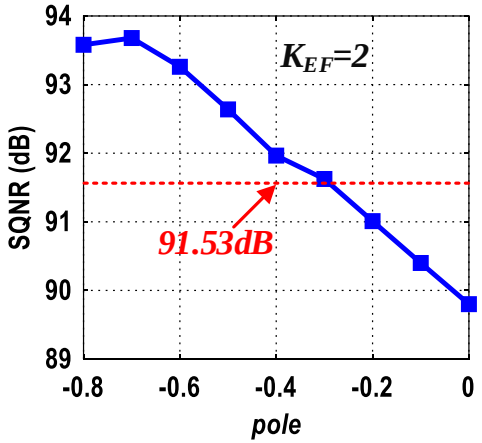
- ✓ If $g=\frac{1-\beta}{A_{RS}\times\beta}$, pole z=0
- ✓ Zero Position(1-β) is Compromise Between Noise Shaping Capability and Capacitor Area of C_{int}
- ✓ Left-Plane Pole is Good for Noise Shaping

Proposed Hybrid Noise-Shaping SAR ADC

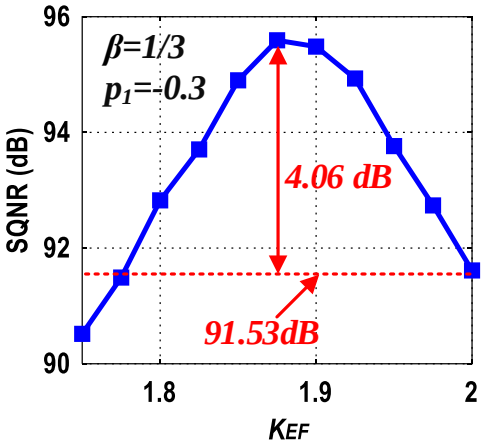
$$NTF=\frac{1-K_{EF}\times FIR(z)}{1+gA_{RS}z^{-1}\times IIR(z)}=\frac{(1-K_{EF}\times(z^{-1}-0.5z^{-2}))\times(1-(1-\beta)z^{-1})}{1-((1-\beta)-\beta gA_{RS})z^{-1}}$$



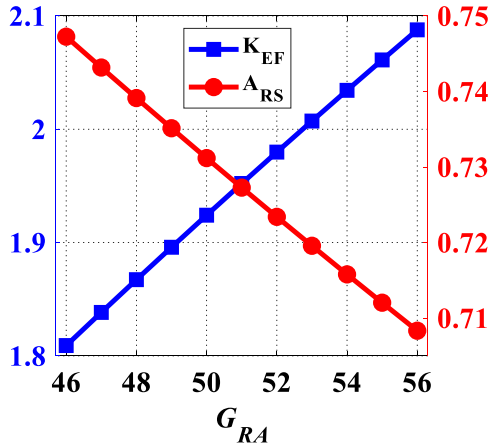
(a)



(b)



(c)

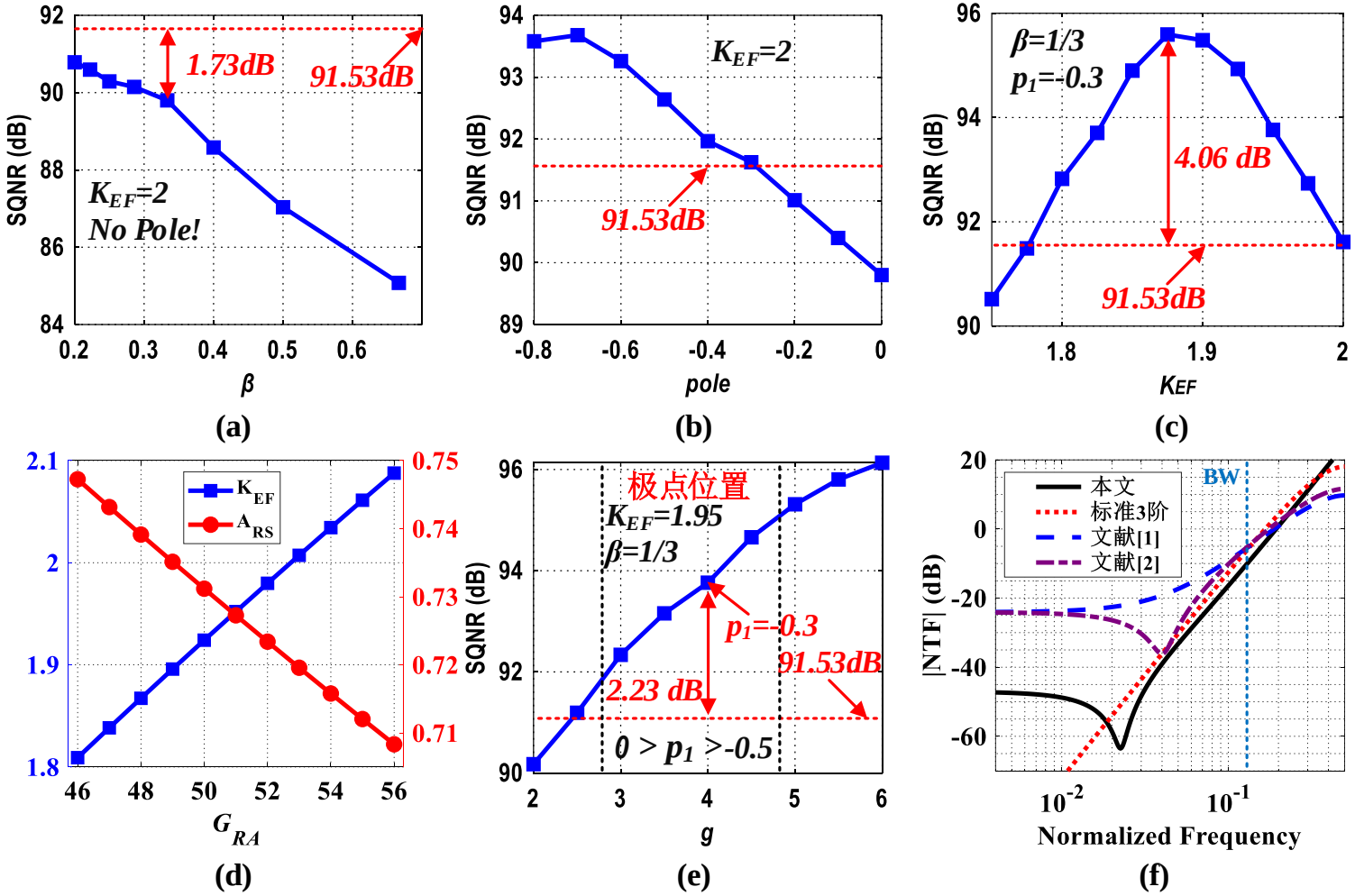


(d)

- ✓ A Pair of Real Zeros Are Changed to Complex Zeros By Adjusting K_{EF} for Better Dynamic Performance
- ✓ Close-loop Gain of RA is a Little Larger to Compensate the Finite Gain of OTA

Proposed Hybrid Noise-Shaping SAR ADC

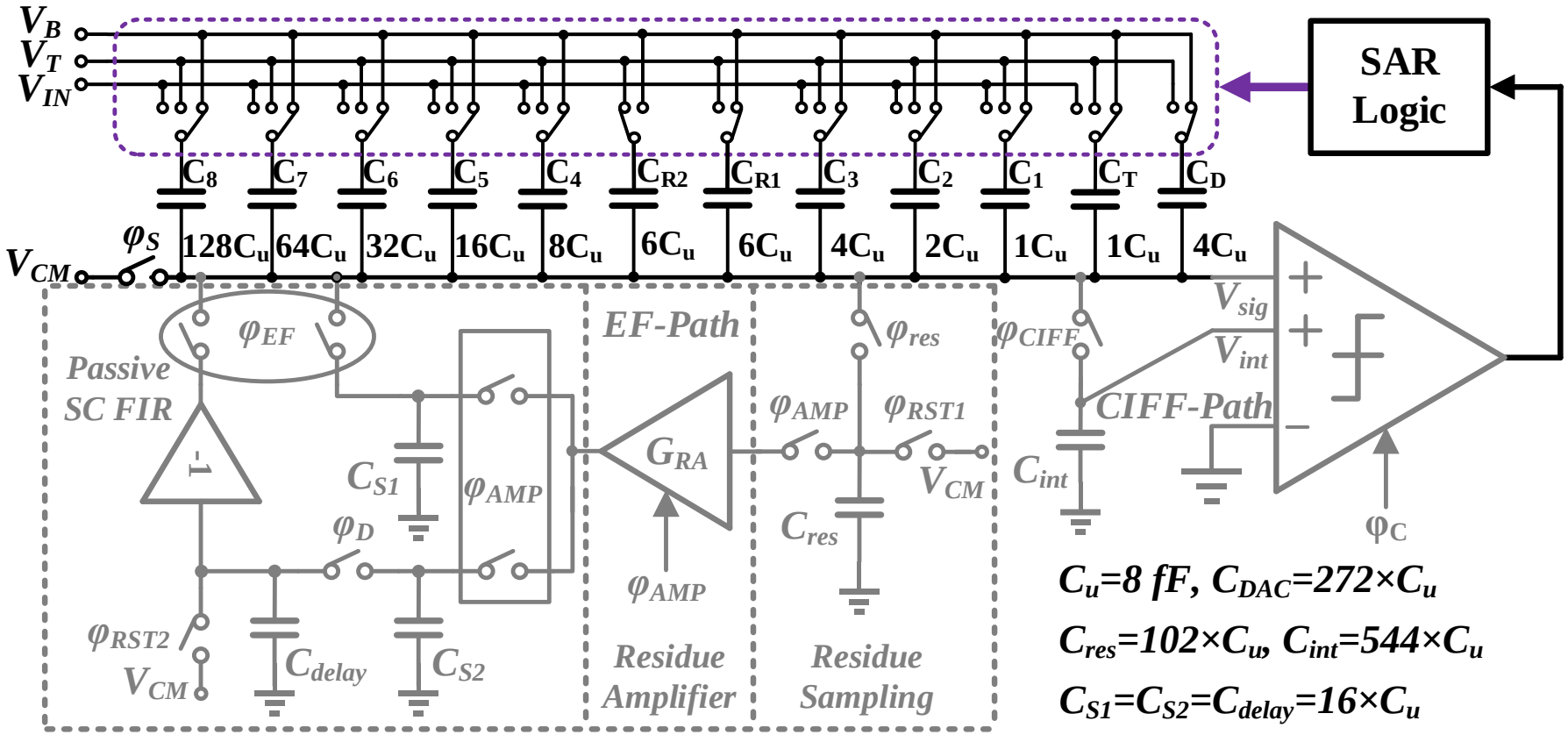
$$NTF=\frac{1-K_{EF}\times FIR(z)}{1+gA_{RS}z^{-1}\times IIR(z)}=\frac{(1-K_{EF}\times(z^{-1}-0.5z^{-2}))\times(1-(1-\beta)z^{-1})}{1-((1-\beta)-\beta gA_{RS})z^{-1}}$$



- ✓ Left-plane Pole z=-0.3 is Realized When Comparator Gain of 4
- ✓ Notch is Found Around BW, Shows Better Noise Shaping Performance

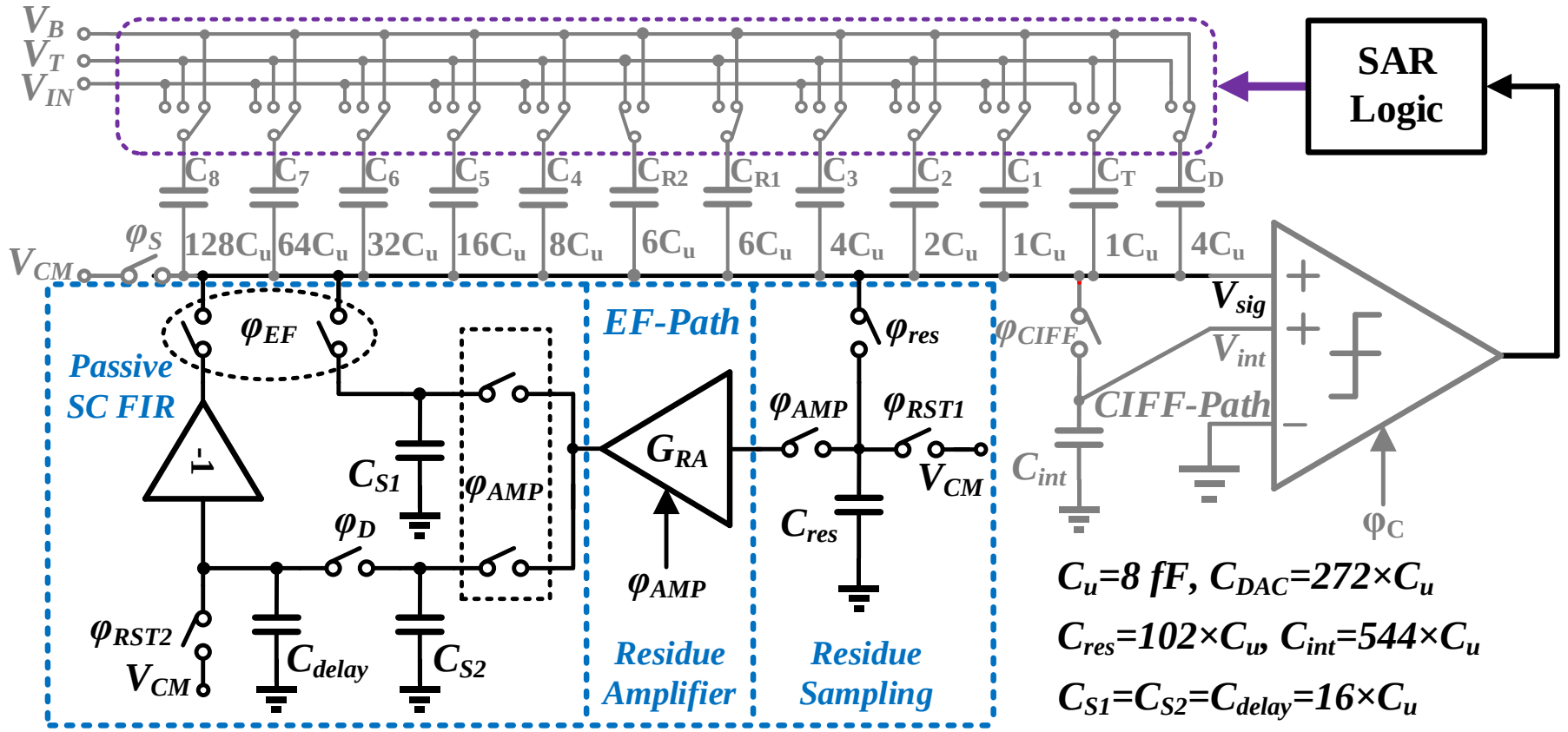
[1] W. Guo. et.al, *ESSCIRC* 2016.
[2] Q. Zhang, *IEEE T-VLSI* 2021.

Proposed Hybrid Noise-Shaping SAR ADC



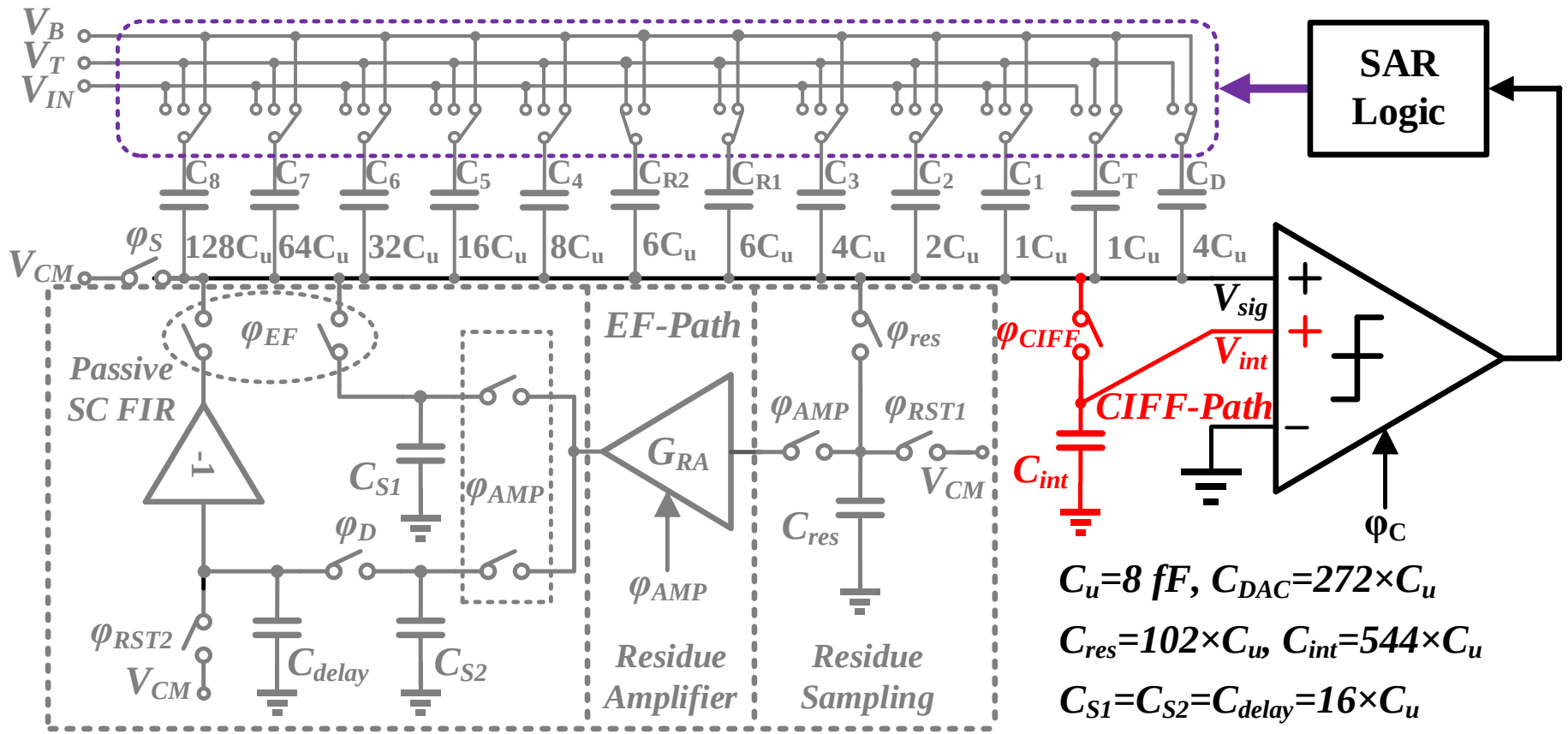
- ✓ 8+2b DAC, C_{R2} and C_{R1} Are Used to Compensate The Filtered Residues From EF Path
- ✓ C_D is Used for Dither， Quantize 2 Times for Different Codes

Proposed Hybrid Noise-Shaping SAR ADC



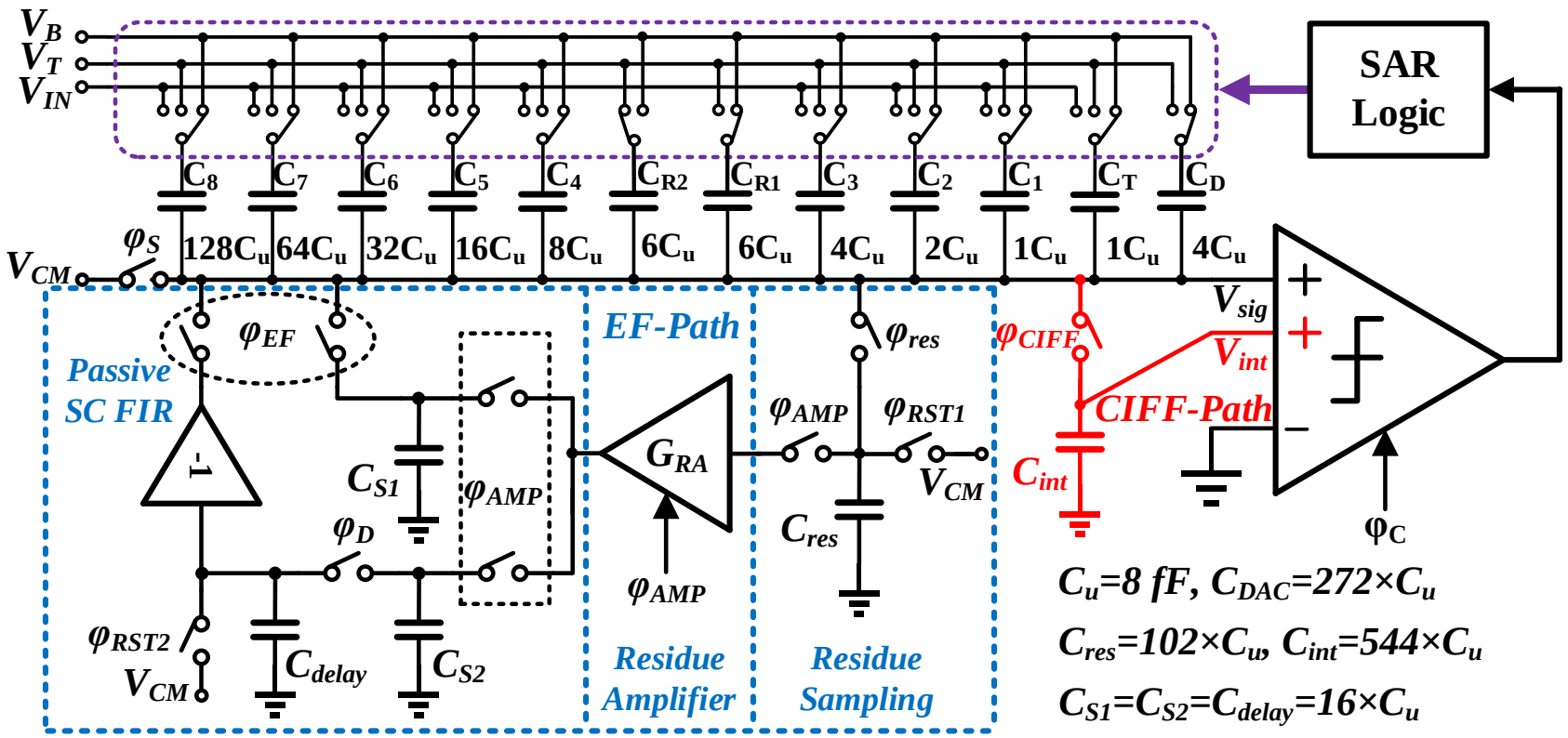
- ✓ EF Path: Residue Sample Cap, RA , Passive SC-Based FIR
- ✓ Close-Loop RA for Accurate Gain

Proposed Hybrid Noise-Shaping SAR ADC



- ✓ CIFF Path is Composed by C_{int} and Comparator Integration Path
- ✓ Gm ratio of Multi-Input Comparator for gain

Proposed Hybrid Noise-Shaping SAR ADC

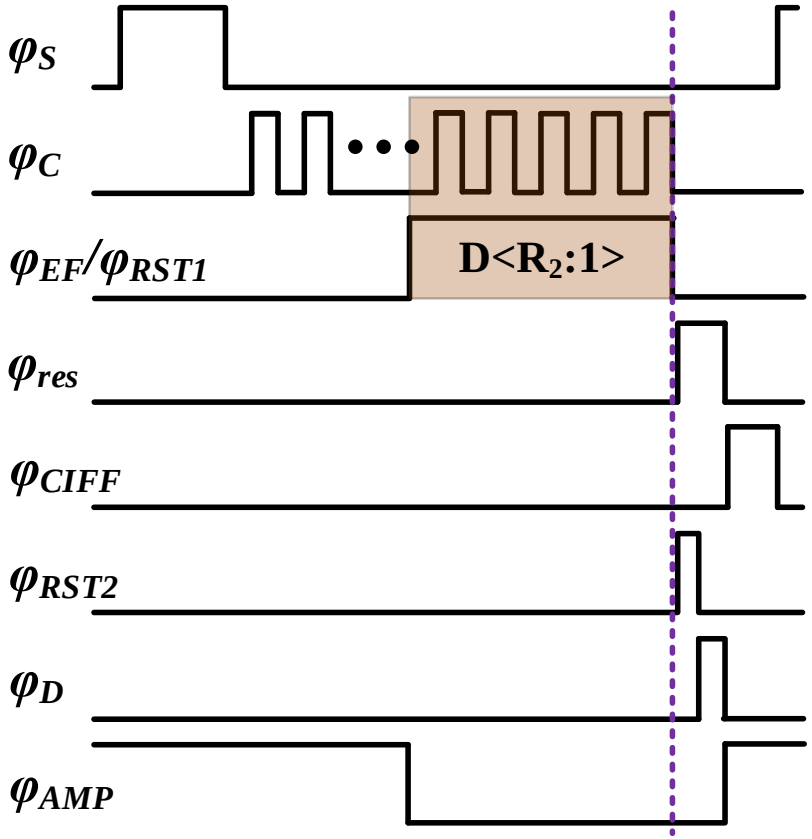


C_u=8 fF, C_{DAC}=272×C_u

C_{res}=102×C_u, C_{int}=544×C_u

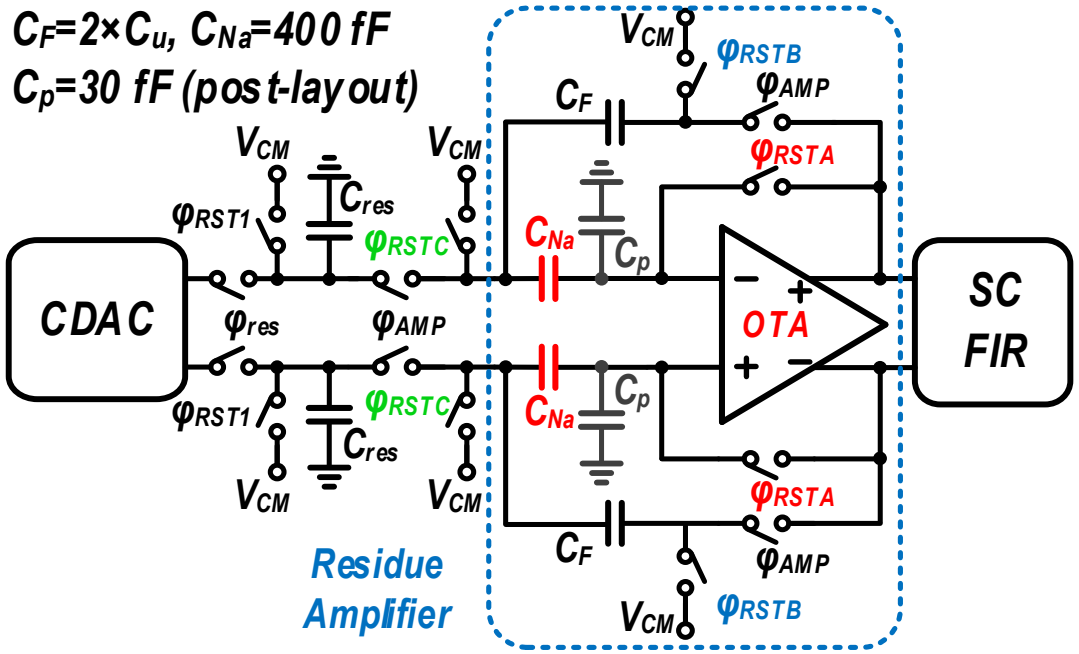
C_{S1}=C_{S2}=C_{delay}=16×C_u

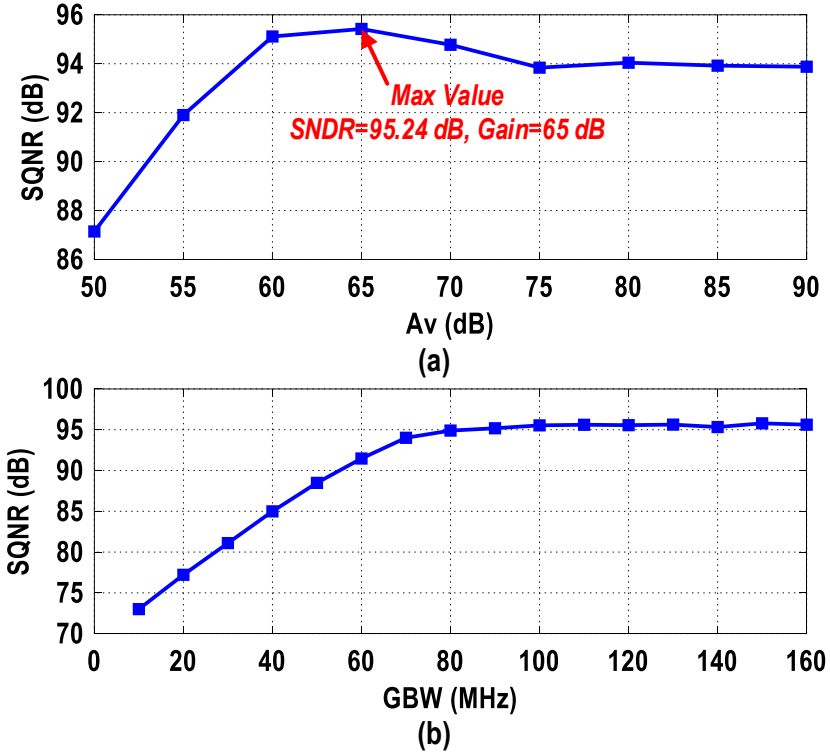
Architecture



Timing

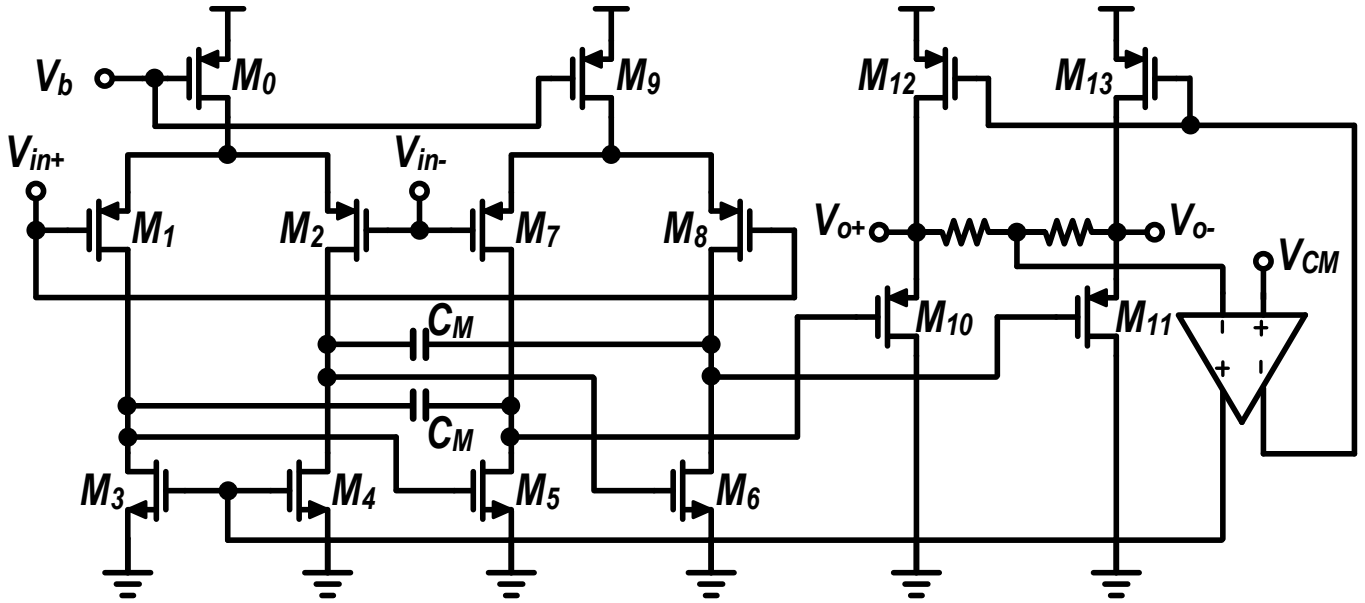
Proposed Hybrid Noise-Shaping SAR ADC

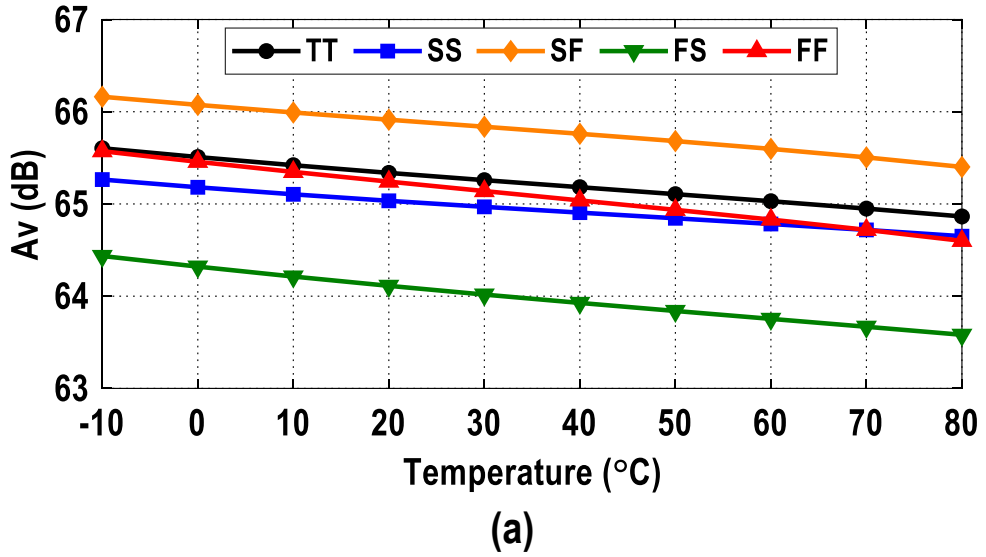




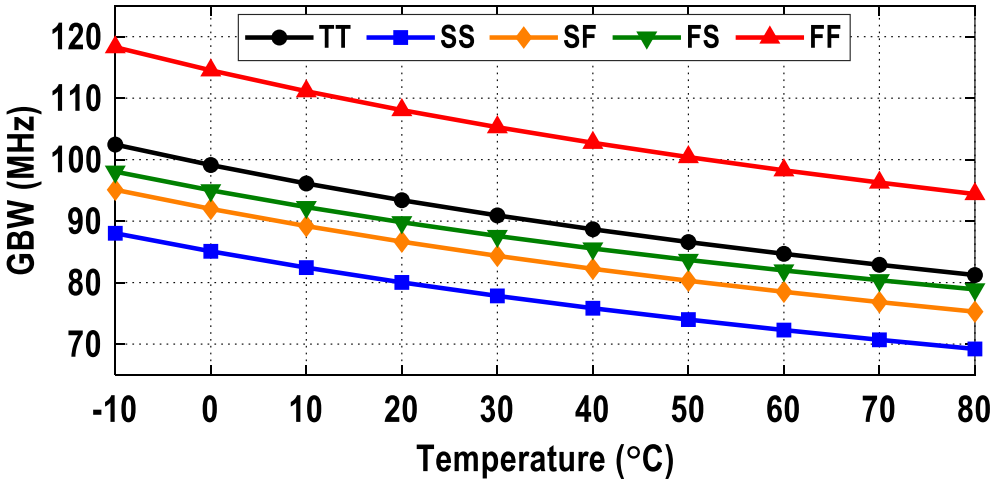
- ✓ IOS is Used to Store the Offset of OTA and Prevent OTA/ADC Saturation
- ✓ Finite Gain Limits EF Path Gain, But not Degrades SQNR
- ✓ RA Works with DAC Sample and Quantize, Reduce the BW Demand

Proposed Hybrid Noise-Shaping SAR ADC





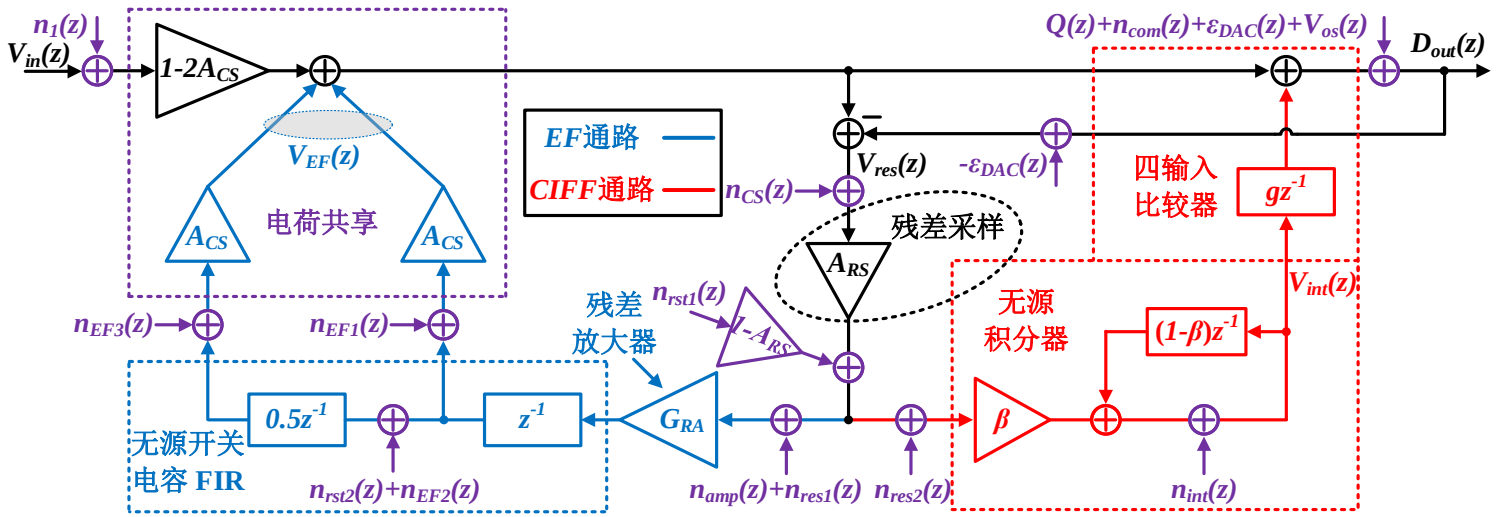
(a)

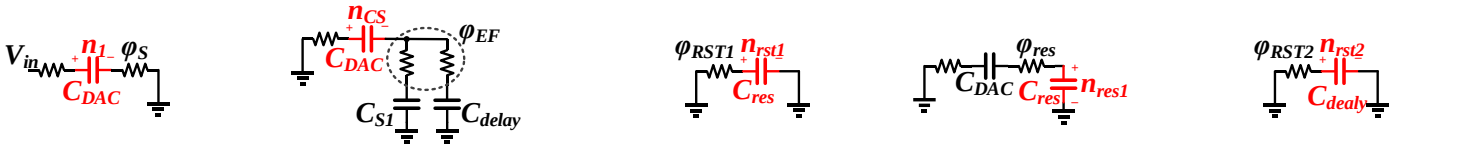


(b)

- ✓ OTA Adopts Feedforward Architecture to Generate Left-plane Zero for GBW Improvement
- ✓ Gain and GBW Satisfy The Requirement under Corners and Temperature

Proposed Hybrid Noise-Shaping SAR ADC





n_1: DAC采样噪声

$$\overline{n_1^2}=\frac{kT}{C_{DAC}}$$

n_{CS}: DAC电荷求和噪声

$$\overline{n_{CS}^2}=\frac{kT}{C_{DAC}}\times\frac{C_{delay}+C_{S1}}{C_{DAC}+C_{delay}+C_{S1}}$$

n_{rst1}: C_{res}复位噪声

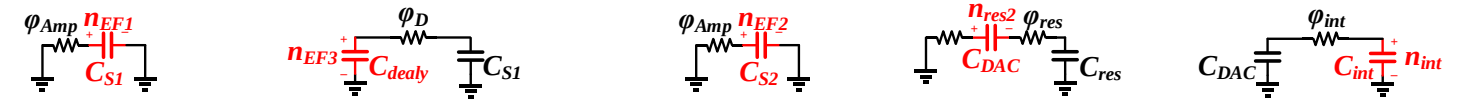
$$\overline{n_{rst1}^2}=\frac{kT}{C_{res}}$$

n_{res1}: C_{res}残差采样噪声

$$\overline{n_{res1}^2}=\frac{kT}{C_{res}}\times\frac{C_{DAC}}{C_{DAC}+C_{res}}$$

n_{rst2}: C_{dealy}复位噪声

$$\overline{n_{rst2}^2}=\frac{kT}{C_{dealy}}$$



n_{EF1}: C_{S1} 采样噪声

$$\overline{n_{EF1}^2}=\frac{kT}{C_{S1}}$$

n_{EF3}: C_{dealy}采样电荷转移噪声

$$\overline{n_{EF3}^2}=\frac{kT}{C_{dealy}}\times\frac{C_{S1}}{C_{dealy}+C_{S1}}$$

n_{EF2}: C_{S2} 采样噪声

$$\overline{n_{EF2}^2}=\frac{kT}{C_{S2}}$$

n_{res2}: C_{DAC}残差采样噪声

$$\overline{n_{res2}^2}=\frac{kT}{C_{DAC}}\times\frac{C_{res}}{C_{DAC}+C_{res}}$$

n_{int}: C_{int}积分噪声

$$\overline{n_{int}^2}=\frac{kT}{C_{int}}\times\frac{C_{int}}{C_{DAC}+C_{int}}$$

$$D_{out}(z)=(1-2A_{CS})\times V_{in}(z)+\varepsilon(z)$$

未整形 $+(1-2A_{CS})\times n_1(z)$

未整形 $+H_{n1}(z)\times[n_{EF1}(z)-n_{EF3}(z)]$

未整形 $+H_{n2}(z)\times[n_{rst2}(z)+n_{EF2}(z)]$

一阶整形 $+H_{n3}(z)\times[n_{amp}(z)+n_{res1}(z)]$

二阶整形 $+H_{n4}(z)\times[A_{RS}n_{CS}(z)+(1-A_{RS})\times n_{rst1}(z)]$

二阶整形 $-H_{n5}(z)\times[\beta n_{res2}(z)+n_{int}(z)]$

三阶整形 $+H_{n6}(z)\times[Q(z)+n_{com}(z)+V_{os}(z)]$

$$H_{n1}(z)=A_{CS}$$

$$H_{n2}(z)=0.5A_{CS}z^{-1}$$

$$H_{n3}(z)=G_{RA}A_{CS}(z^{-1}-0.5z^{-2})$$

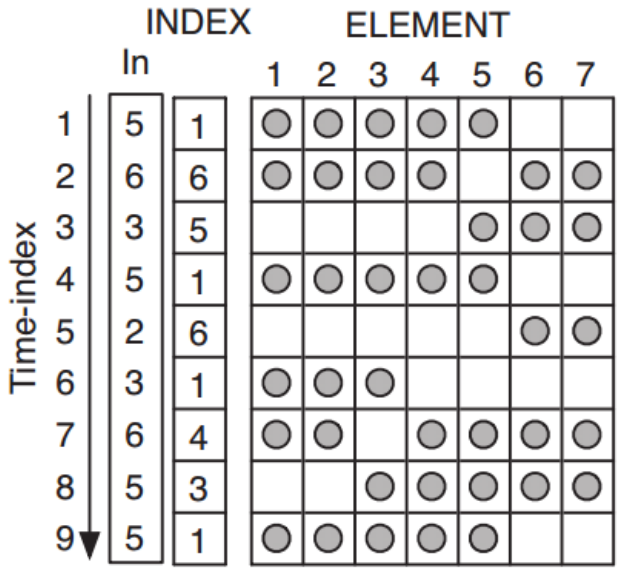
$$H_{n4}(z)=\eta\{[G_{RA}A_{CS}(z^{-1}-0.5z^{-2})]\times[1-(1-\beta)z^{-1}]+\beta gz^{-1}\}$$

$$H_{n5}(z)=\eta g[1-A_{RS}G_{RA}A_{CS}(z^{-1}-0.5z^{-2})]$$

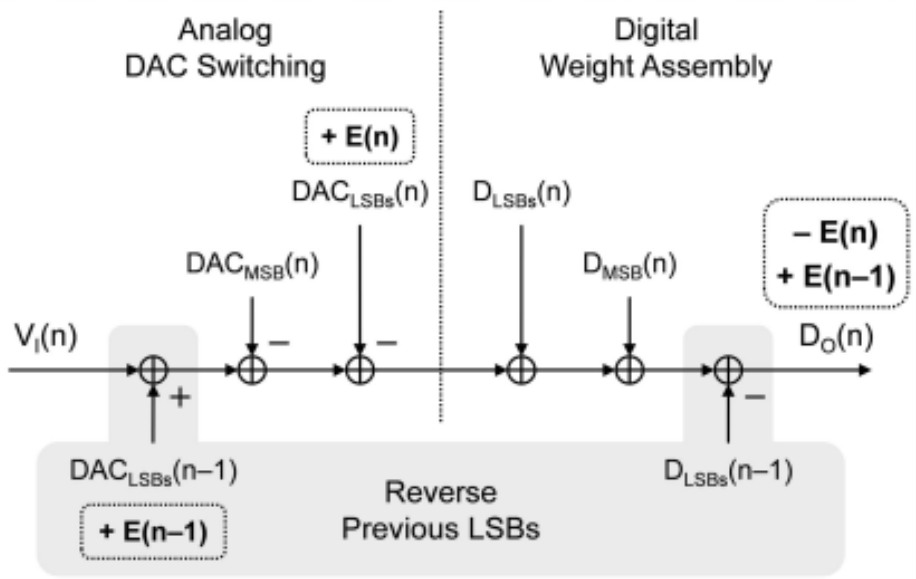
$$H_{n6}(z)=\eta[1-A_{RS}G_{RA}A_{CS}(z^{-1}-0.5z^{-2})]\times[1-(1-\beta)z^{-1}]$$

$$1/\eta=1-[(1-\beta)-A_{RS}\beta g]z^{-1}$$

Foreground Capacitor Mismatch Calibration

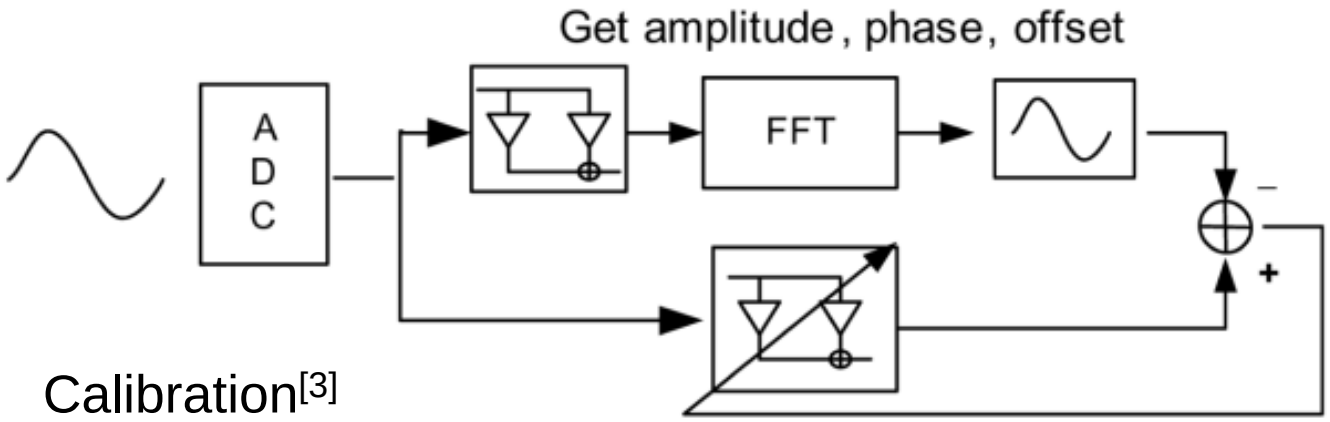


DWA[1]



MES[2]

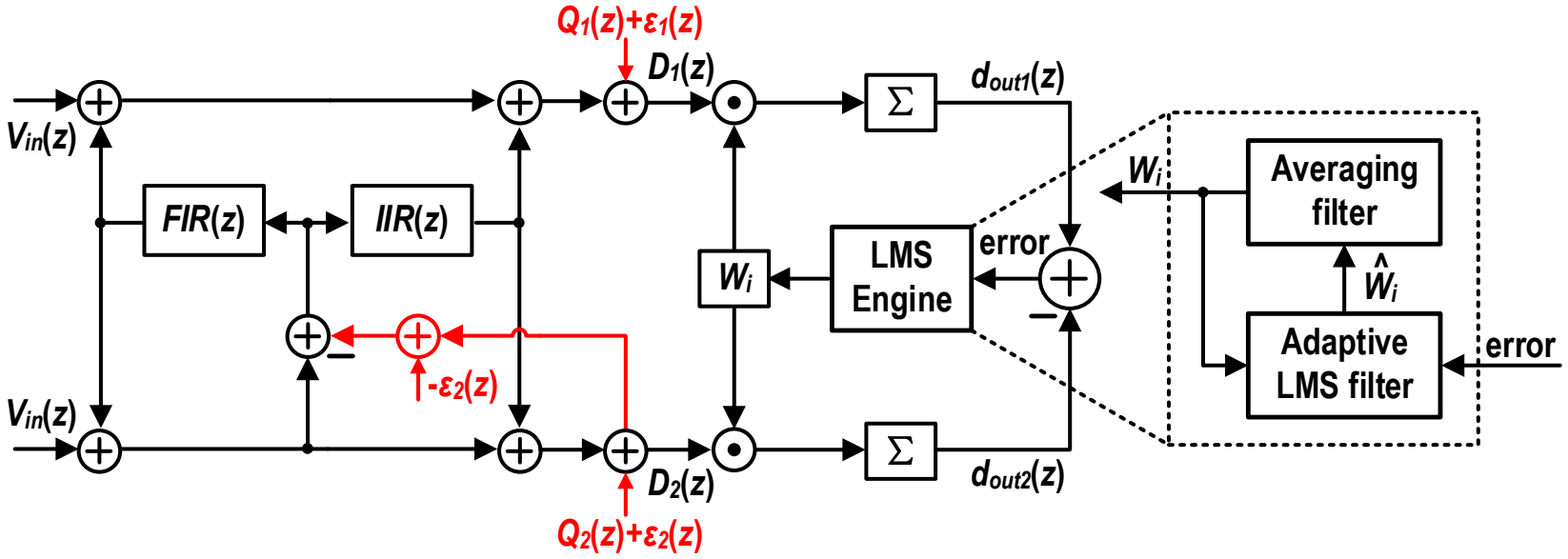
- DWA: The mismatch error has been converted into white noise.
- MES: The usable input range has been greatly reduced.
- Calibration: FFT processor requires a lot of multipliers, which increases the complexity of on-chip integration.



Calibration[3]

[1] D. Lee and T. Kuo, IEEE TCASII, 2007.
[2] Y. Shu, et al., IEEE JSSC, 2016.
[3] S. M. Chen and R. W. Brodersen, IEEE JSSC, 2006.

Foreground Capacitor Mismatch Calibration



$$d_{out1}(z) = V_{in}(z) + Q_1(z) - Q_2(z) \times \frac{FIR(z) + IIR(z)}{1 + IIR(z)} + \varepsilon_1(z),$$

$$d_{out2}(z) = V_{in}(z) + Q_2(z) \times \frac{1 - FIR(z)}{1 + IIR(z)} + \varepsilon_2(z).$$

$$error = \underbrace{\left(Q_1(z) - Q_2(z)\right)}_{\text{Quantization noise}} + \underbrace{\left(\varepsilon_1(z) - \varepsilon_2(z)\right)}_{\text{Mismatch}}$$

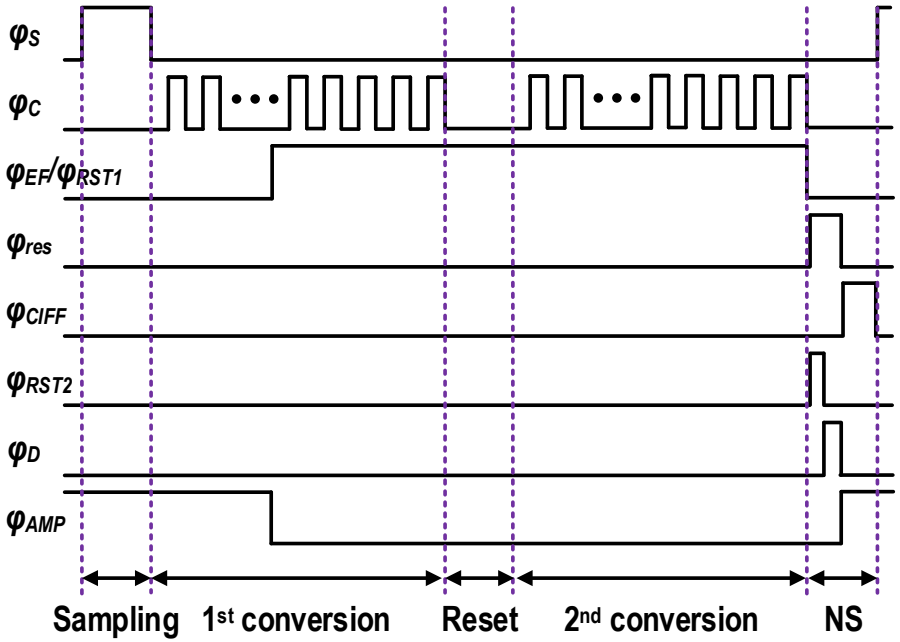
$$\hat{W}_i[n+1] = W_i[n] - \mu_w error[n]\left(D_{1,i}[n] - D_{2,i}[n]\right),$$

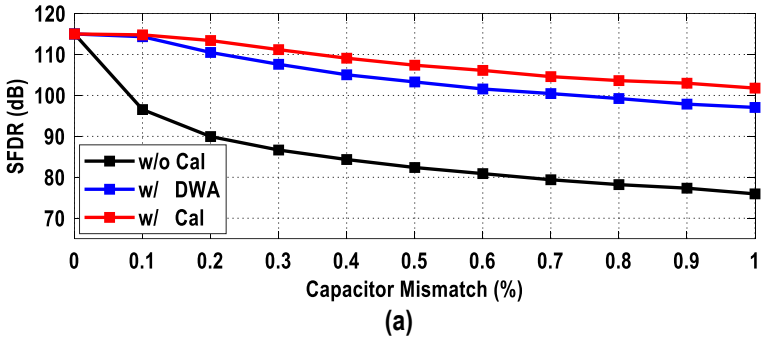
$$W_i[n+1] = \frac{\sum_{i=0}^{M-1} \hat{W}_i[n+1-i]}{M}.$$

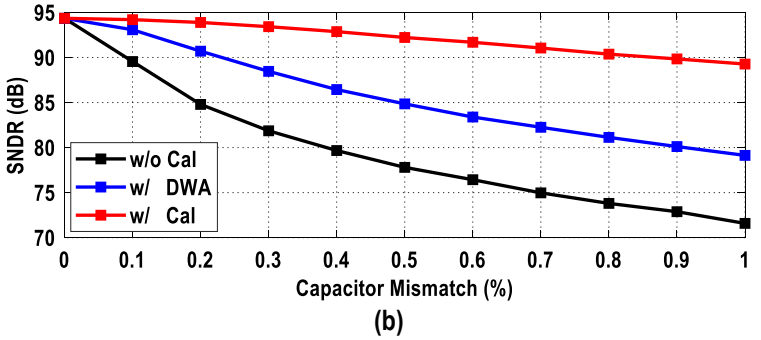
Suppress Quantization noise

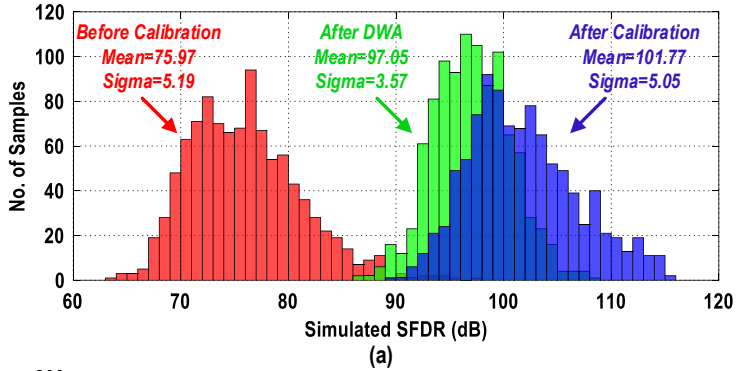
- ✓ LMS Based Algorithm, Each Analog Sample Should Be Digitized Twice During The Foreground Calibration Phase.
- ✓ Averaging Filter Used to Suppress The Interference From Quantization Noise.
- ✓ No Multiplier Needed, Low Hardware Cost .

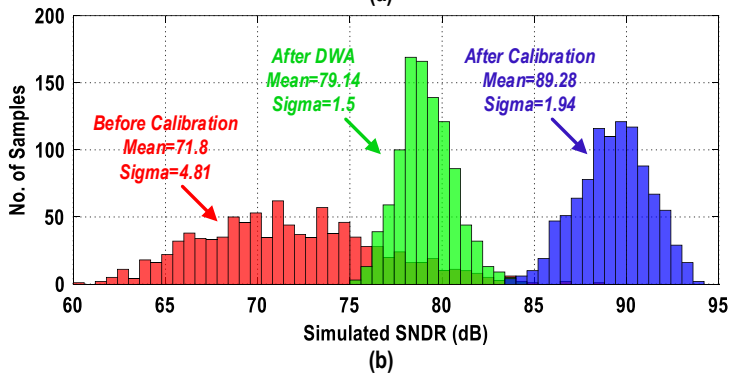
Foreground Capacitor Mismatch Calibration

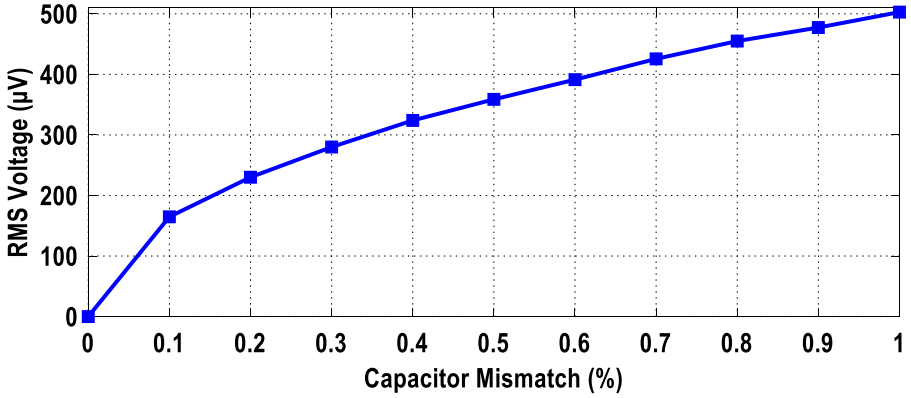






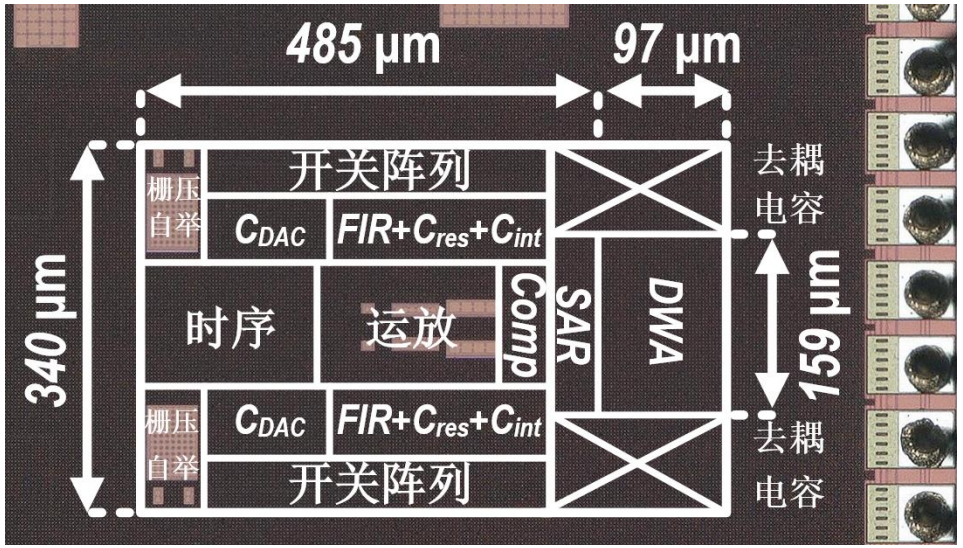






- ✓ The capacitor mismatch will directly appear in digital output and can not be shaped by NS loop.
- ✓ The quantization noise generated at twice conversion shows a strong correlation. As mismatch error increase, this dependence becomes weaker.

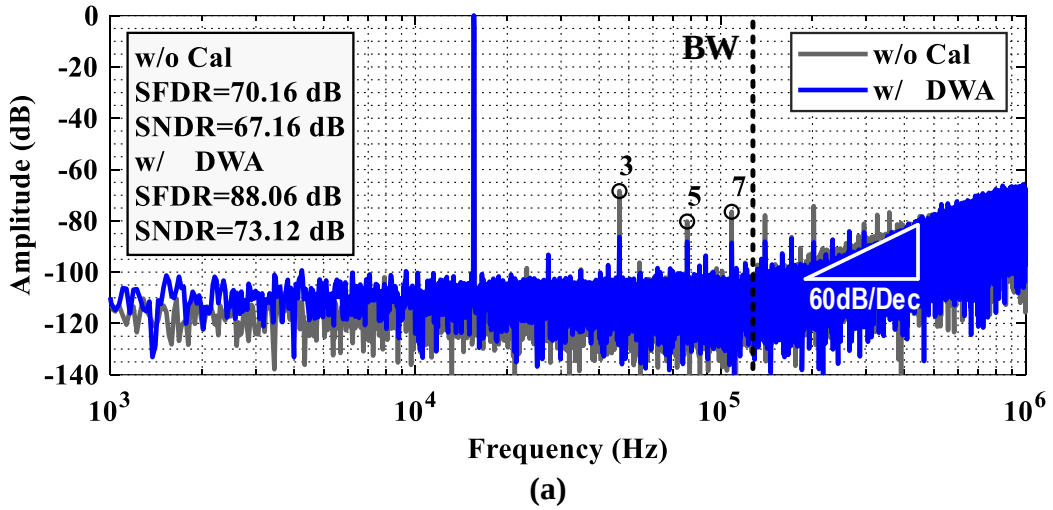
Measurement Results

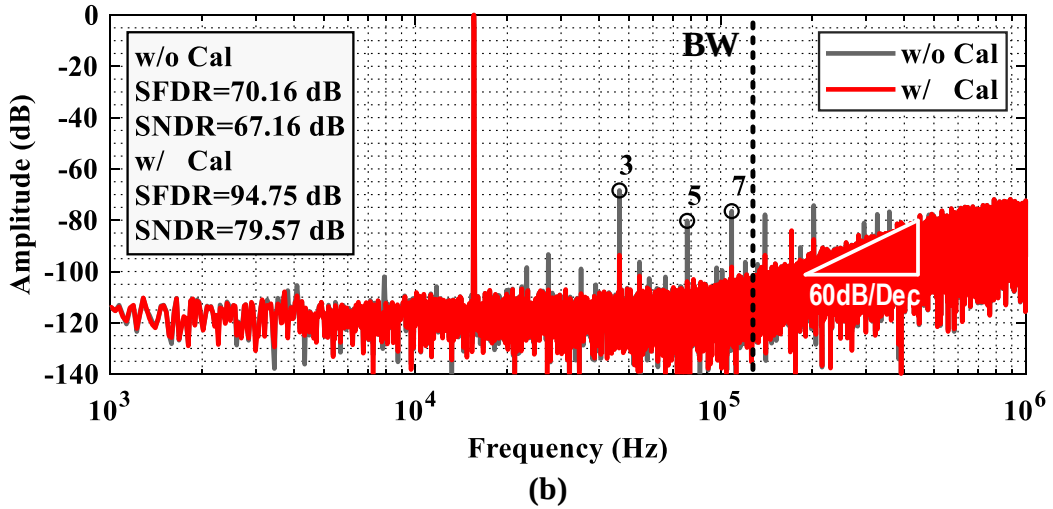


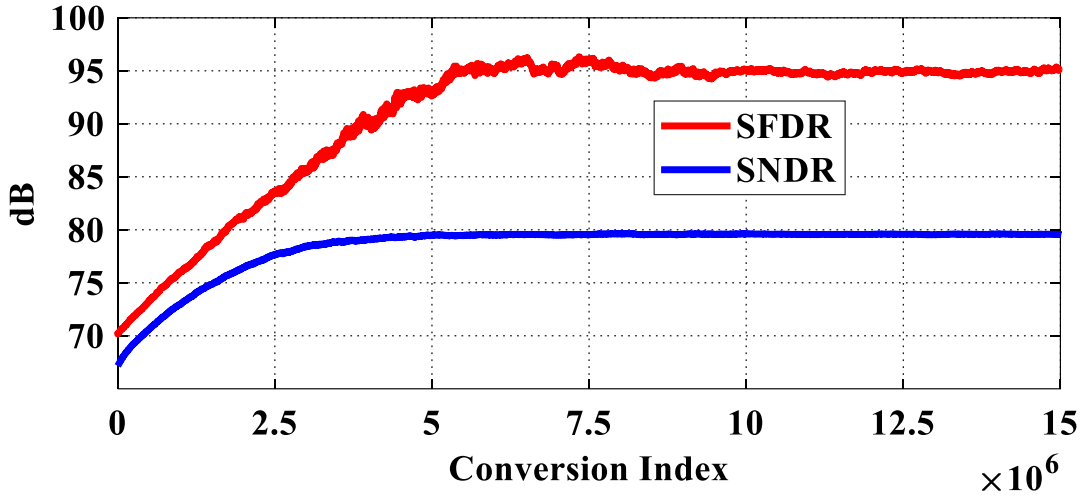
Noise Contribution	Noise power	Percentage
Input Sampling	$(22.6\ \mu V)^2$	10%
Quantization	$(15.2\ \mu V)^2$	4.5%
Comparator	$(3.1\ \mu V)^2$	0.2%
Residue Sampling	$(54.1\ \mu V)^2$	57.6%
Residue Amplifier	$(35.5\ \mu V)^2$	24.8%
SC FIR	$(11.6\ \mu V)^2$	2.65%
SC IIR	$(3.6\ \mu V)^2$	0.25%

- ✓ Fabricated in 0.13μm CMOS Process.
- ✓ Core Area 485×340 μm^2 .
- ✓ MOM Capacitors are Adopted.
- ✓ Foreground Calibration Performed on FPGA.
- ✓ Power Consumption 96μW Under 1.2-V supply.
- ✓ Operating at 2-MHz With an Oversampling Ratio (OSR) of 8 and BW 125kHz.

Measurement Results

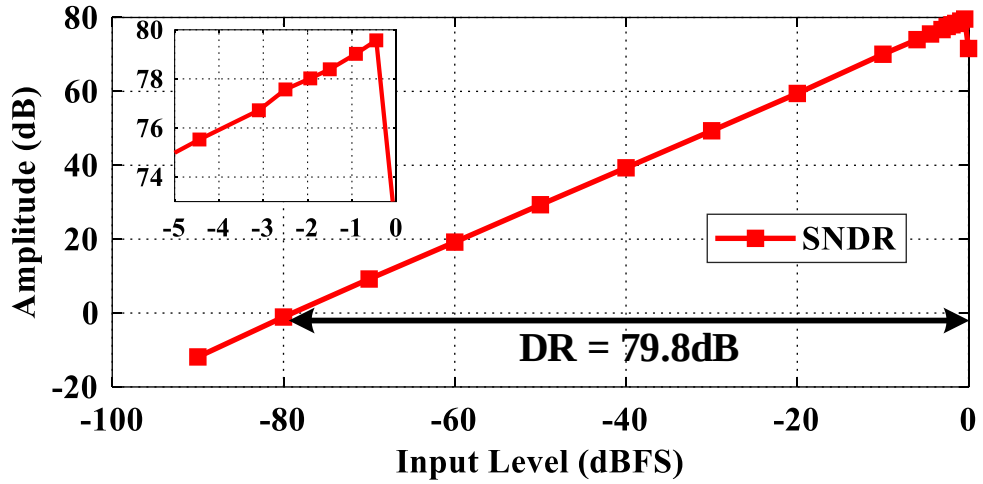


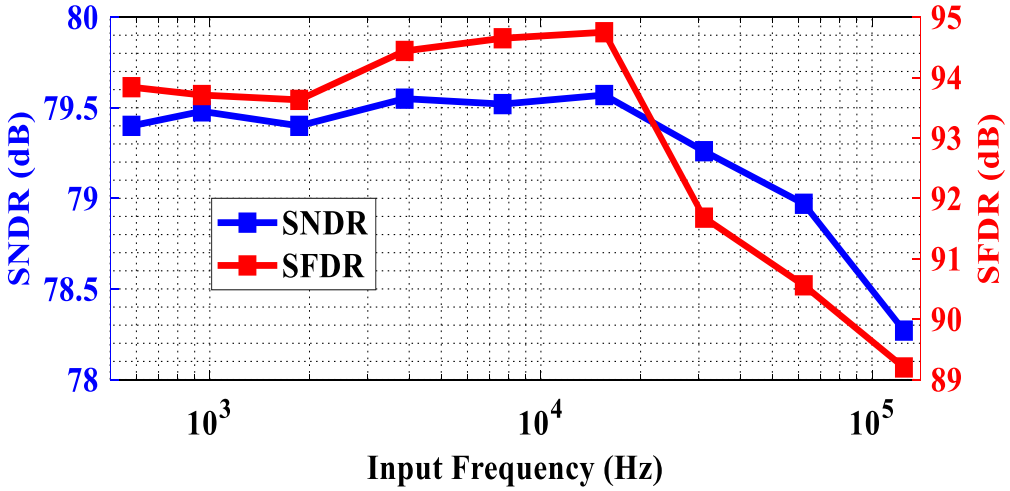


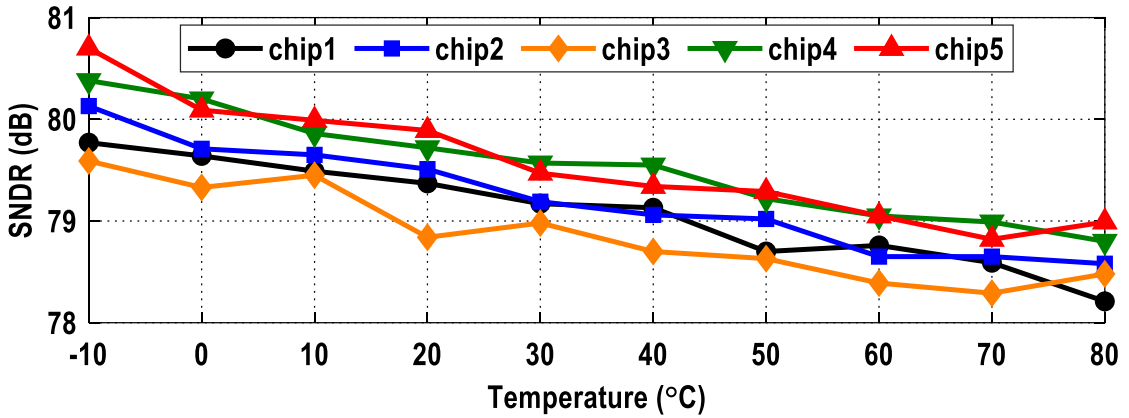


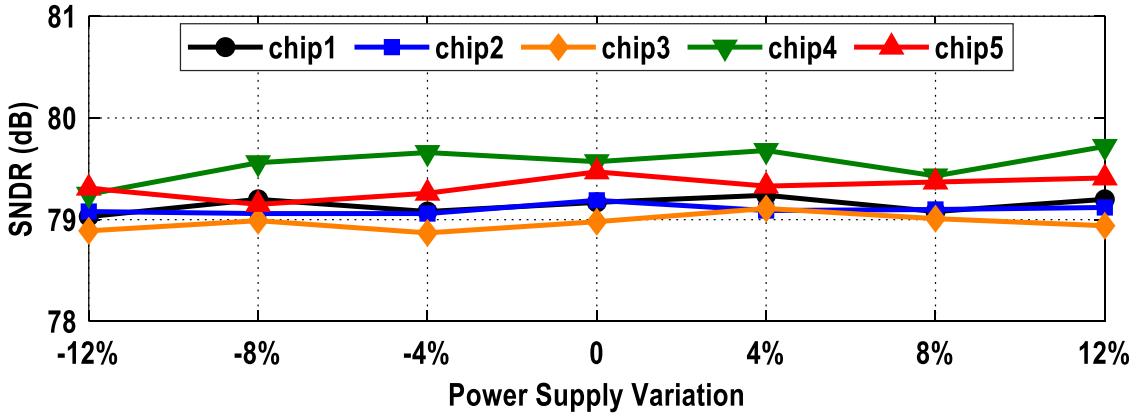
- ✓ 3rd-Order Shaping of 60 dB/dec.
- ✓ DWA Suppresses The Distortions and Spurs, but Increases The Noise Floor.
- ✓ With Digital Foreground Calibration, Harmonics Across The BW Are Suppressed to -90 dB Without Noise Deterioration.
- ✓ The Convergence Speed is Strongly Related to The Averaging Filter.

Measurement Results









- ✓ DR =79.8dB
- ✓ SNDR > 78dB vs f_{in}
- ✓ All Measured Chips Keep Performance Over Supply and Temperature Variation

Measurement Results

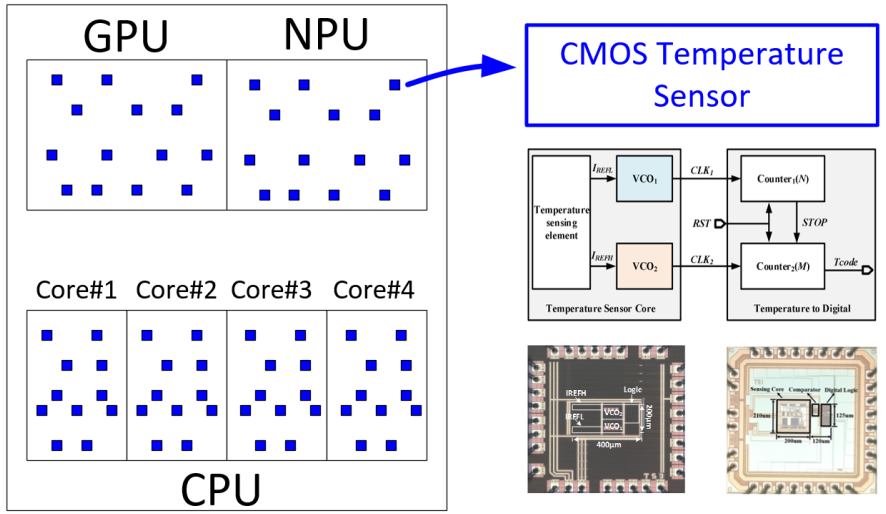
	JSSC'18 S. Li	JSSC'19 H. Zhuang	JSSC'20 L. Jie	JSSC'20 X. Tang	TVLSI'21 Q. Zhang	JSSC'21 T. Wang	This Work
Architecture	EF	CIFF	Cascade-EF	CIFF	CIFF	EF-CIFF	EF-CIFF
NTF Order	2	2	4	2	2	3	3
Insensitive PVT	No	Yes	Yes	Yes	Yes	Yes	Yes
Mismatch Cal. Complexity	Hard	Hard	Hard	Hard	DWA	Hard	Simple
Amplifier	Dynamic	Passive	Op-amp	Dynamic	Passive	Dynamic	Op-amp
CMOS (nm)	40	40	28	40	130	65	130
Supply	1.1	1.1	1	1.1	1.2	1.1	1.2
Resolution (bit)	9	9	8	10	9	10	8
Fs (MS/s)	10	8.4	2	10	2	10	2
OSR	8	16	10	8	8	8	8
BW (kHz)	625	262	100	625	125	625	125
DR (dB)	80.5	N/A	89	85.5	79.1	--	79.8
SNDR (dB)	79	78.4	87.6	83.8	78.69	84.8	79.57
ENOB (bit)	12.83	12.73	14.25	13.62	12.78	13.79	12.93
SFDR (dB)	89	90	102.8	94.3	92.9	103	94.75
Power (μW)	84	107	120	107	59.9	119	96
FoMs [#] (dB)	178	171	176.8	181.5	171.9	182	170.7

Conclusions

- ✓ A Third-Order NS-SAR ADC That Leverages a Hybrid Error Control Scheme was Proposed.
- ✓ The Prototype Achieved 13bit ENOB With FoMs of 170dB.
- ✓ Dither-Based Foreground Capacitor Calibration is Proposed and Realized for NS-SAR ADC in This Paper.

Research Interests

高精度nW级片上CMOS温度传感器



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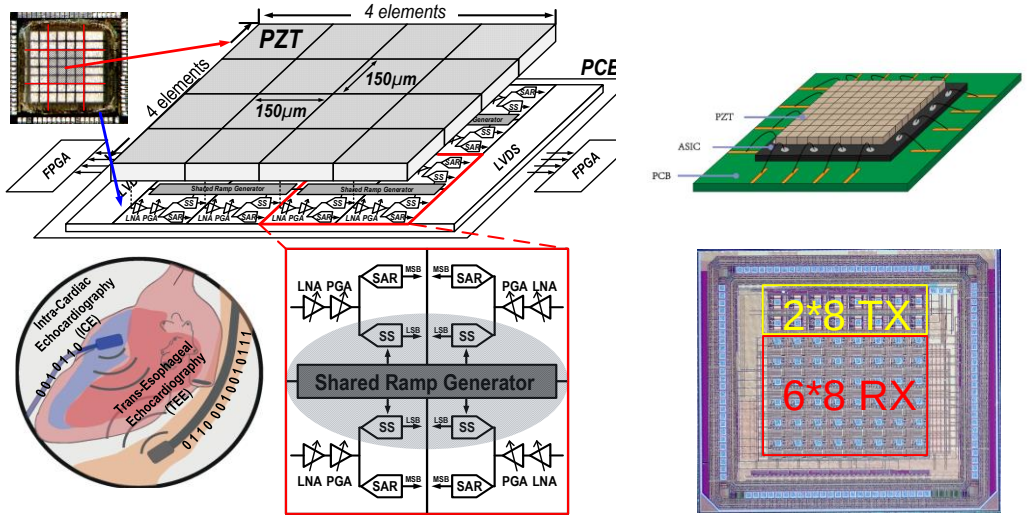
超声医学成像前端专用集成电路



[**Jing Li. et.al**, **2019 *Symposium on VLSI Circuits***, 2019]

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Thank You For Your Attention !