Magnetic-Tuning Technique for CMOS Millimeter-Wave and Terahertz Signal Generation

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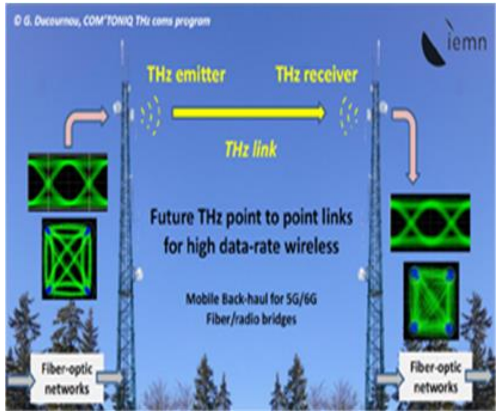
Outline

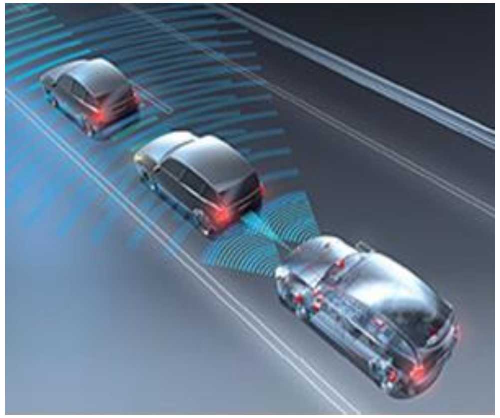
- **Background**
- **Magnetic-Tuning Mm-Wave/THz Oscillators**
- **Mm-Wave/THz Signal Generation System**
- **Conclusion**

Background

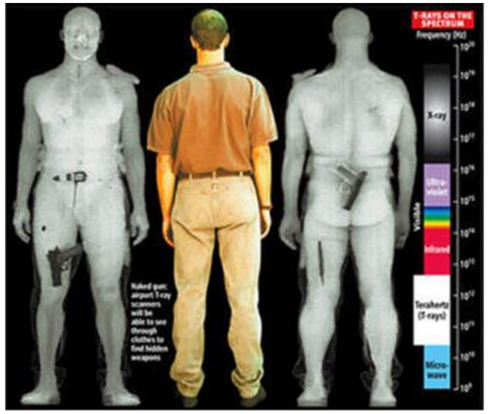
- Mm-Wave/sub-THz frequency band (30 GHz ~ 300 GHz) can be used for various emerging applications
  - Speed of wireless link → Spectrum bandwidth (~10 GHz), modulation scheme (16QAM, PN < -90 dBc/Hz at 1-MHz offset)
  - Resolution and sensitivity of spectroscopy/hyperspectral imaging → Frequency bandwidth (~50 GHz), good signal purity



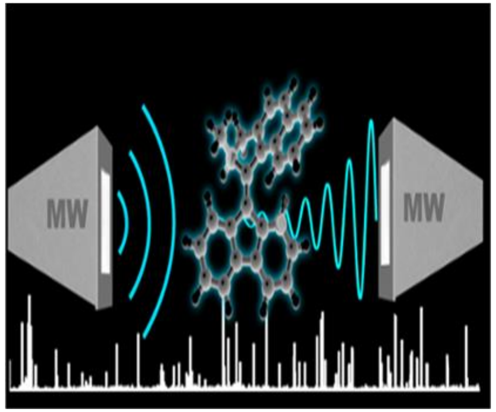
Communication



Vehicular Radar



Passive Imaging



Spectroscopy

Challenges of Silicon-Based Mm-Wave/THz Integration

- Low f_{max} of transistor (e.g. < 220 GHz in 65nm CMOS) → Limited oscillation frequency and amplitude
- Low quality factor of varactors (< 3 at 100 GHz) → Degrade phase noise and output power of oscillators
- Dominated parasitic capacitance → Limited frequency tuning range (< 10% at 100 GHz)
- High loss/coupling of interconnection → Degrade signal power
- Challenging to design and model of a multi-coil transformer → Less accurate and more sensitive → Directly affect the performance

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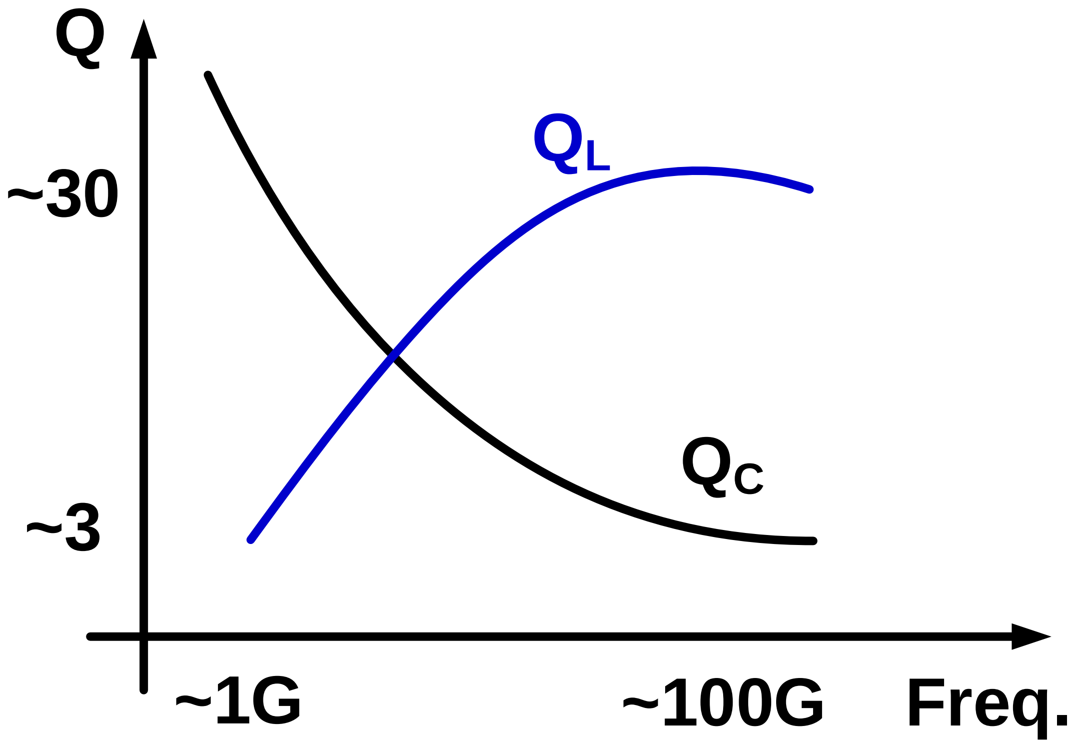
Frequency Tuning



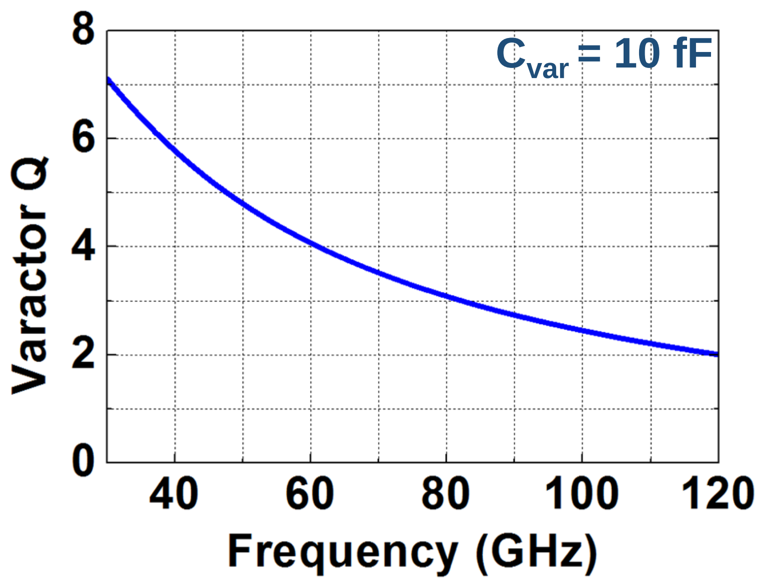
$$Q_L \sim \frac{\omega L}{R_S}$$

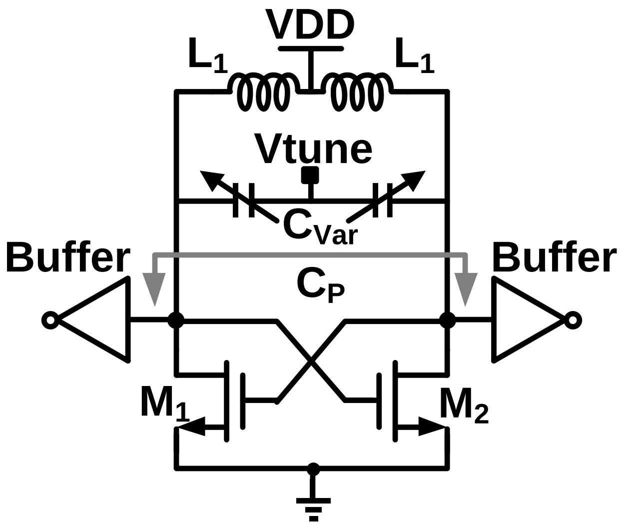
$$Q_C \sim \frac{1}{\omega R_S C}$$

- Tuning would inevitably degrade performance
- At low RF frequencies, $Q_L << Q_C$ → Tuning capacitors
- At high mm-Wave frequencies, $Q_L >> Q_C$ → Tuning inductors and transformers

Existing Mm-Wave Oscillators-Varactors

- Frequency↑ → Q_V↓ → e.g. minimum Q_V is 2.5 at 100 GHz
- Parasitic is relatively large compared to the tuned varactors
- Varactors size↑ for tuning range↑ → Degrade phase noise → Need larger negative-g_m and P_{DC}↑ → Parasitic↑ → Limit the tuning range and maximum f_{osc}





Conventional mm-Wave VCO

@100 GHz

W/L = 12μm/60nm

C_P = 20 fF

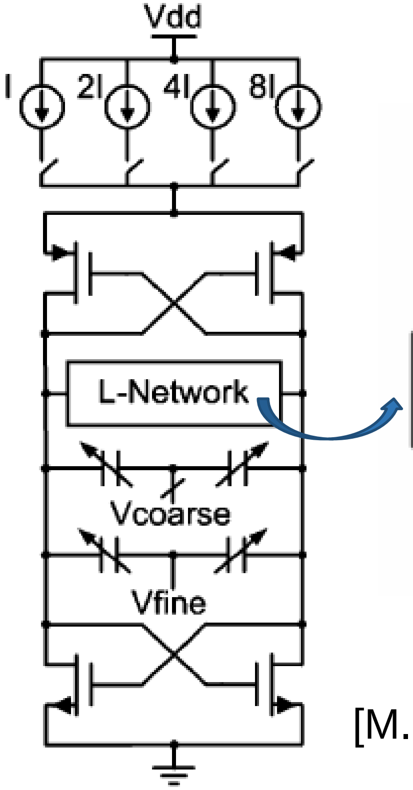
C_{var} = 4-to-10 fF

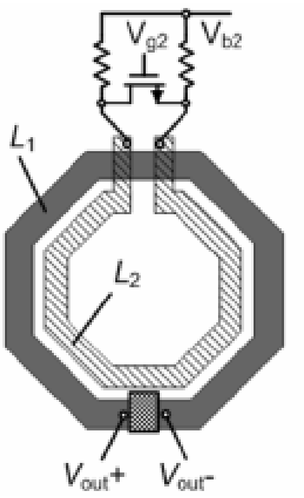
TR = 10.3%

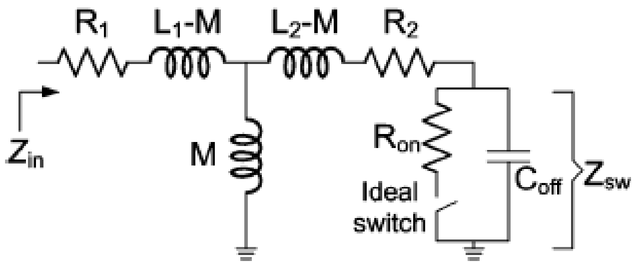
Tank Q_T = 2

Existing Coarse-Magnetic-Tuning Oscillator

- Magnetic tuning by switching on/off extra coupled coils → Coarsely tuned the effective inductance of primary → Wide tuning range







$$L_{\mathrm{eq,on}} \approx L_1 - \frac{M^2}{L_2}$$

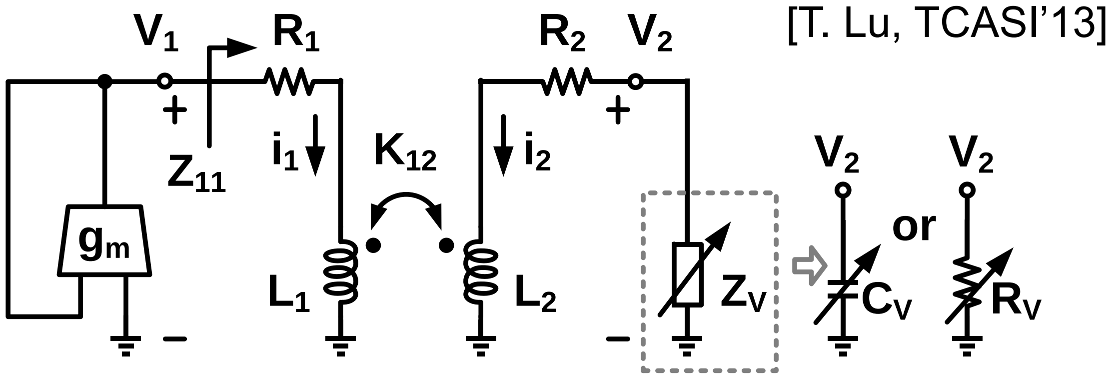
$$L_{\mathrm{eq,off}} \approx L_1 - \frac{\omega M^2}{\omega L_2 - (\omega C_{\mathrm{off}})^{-1}}$$

[M. Demirkan, JSSC'08]

X Low Q_V varactors/capacitors are still used → Worse at high mm-Wave frequencies

Fine Magnetic Tuning with Loaded Component

- Fine magnetic tuning by varying loaded resistor → Remove varactors → Improve tank Q



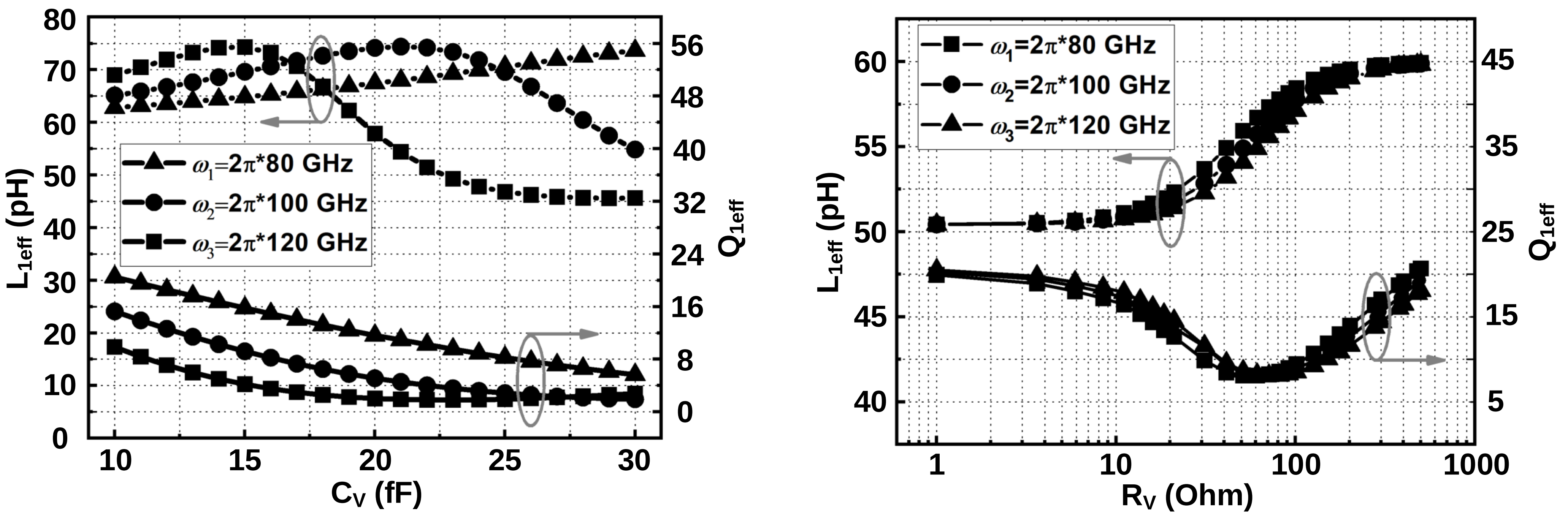
$$Z_{11}(j\omega) = R_1 + j\omega L_1 + \frac{\omega^2 M^2}{R_2 + j\omega L_2 + Z_V}$$

$$L_{1eff} = L_1 - \frac{\omega^2 M^2 L_2}{(R_2 + R_V)^2 + \omega^2 L_2^2}$$

$$R_{1eff} = R_1 + \frac{\omega^2 M^2 (R_2 + R_V)}{(R_2 + R_V)^2 + \omega^2 L_2^2}$$

Loaded Variable resistor R_V

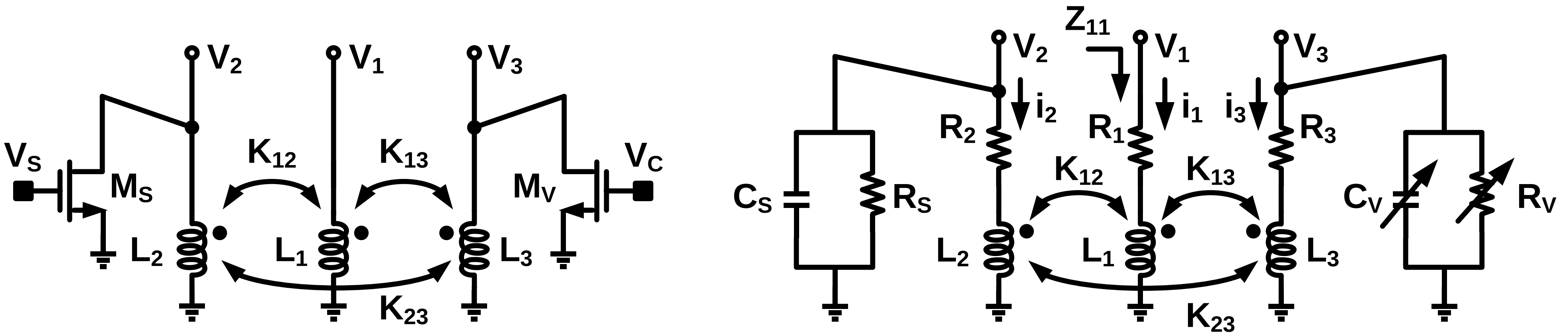
Fine Magnetic Tuning with Loaded Component



- The L_{1eff} and tank Q_{1eff} tuned by a loaded variable R_V is not sensitive to operation frequencies → More attractive for fine magnetic tuning
- A variable resistor R_V can be realized by using a continuously tuned transistor

Triple-coil TF with Coarse and Fine Magnetic Tuning

- M_S on/off for coarse tuning → Dual-band → Wider tuning range
- M_V is tuned continuously → Continuous tuning of L_1 for fine tuning → Remove varactors → Tank Q↑

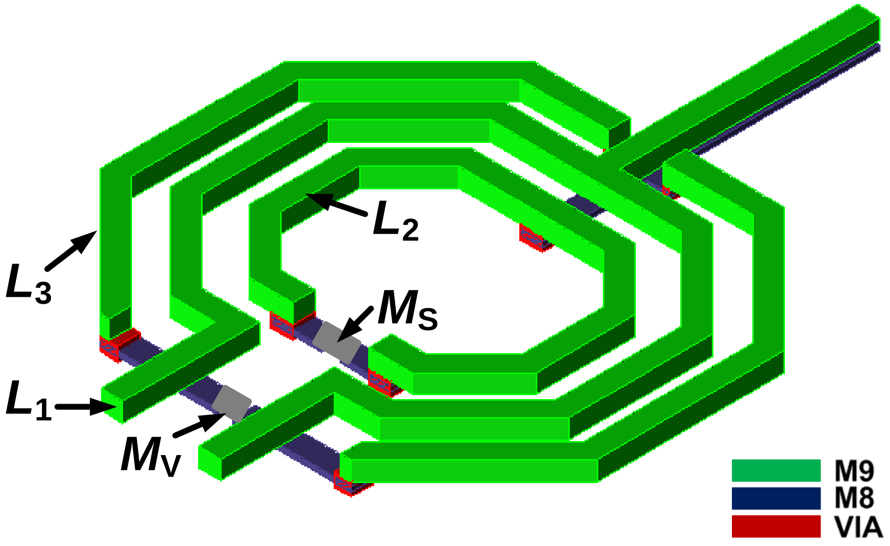


[X. Liu, JSSC'21]

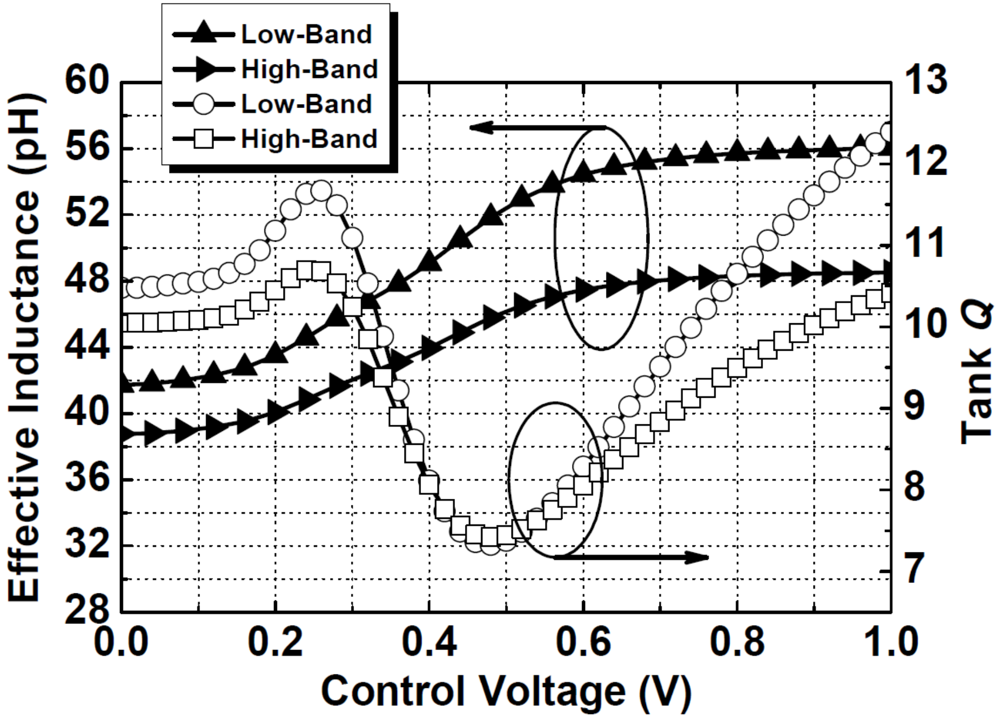
$$L_{1\text{eff}} = L_1 - \frac{\omega^2 M_{12}^2 (L_2 - \alpha R_S C_S)}{(R_2+\alpha)^2 + \omega^2 (L_2 - \alpha R_S C_S)^2} - \frac{\omega^2 M_{13}^2 (L_3 - \beta R_V C_V)}{(R_3+\beta)^2 + \omega^2 (L_3 - \beta R_V C_V)^2}$$

EM Simulation of the Proposed Tank

- Tank QT improved from 2 to 7 at 100 GHz
- Effective inductance change corresponding to tuning range of >15%



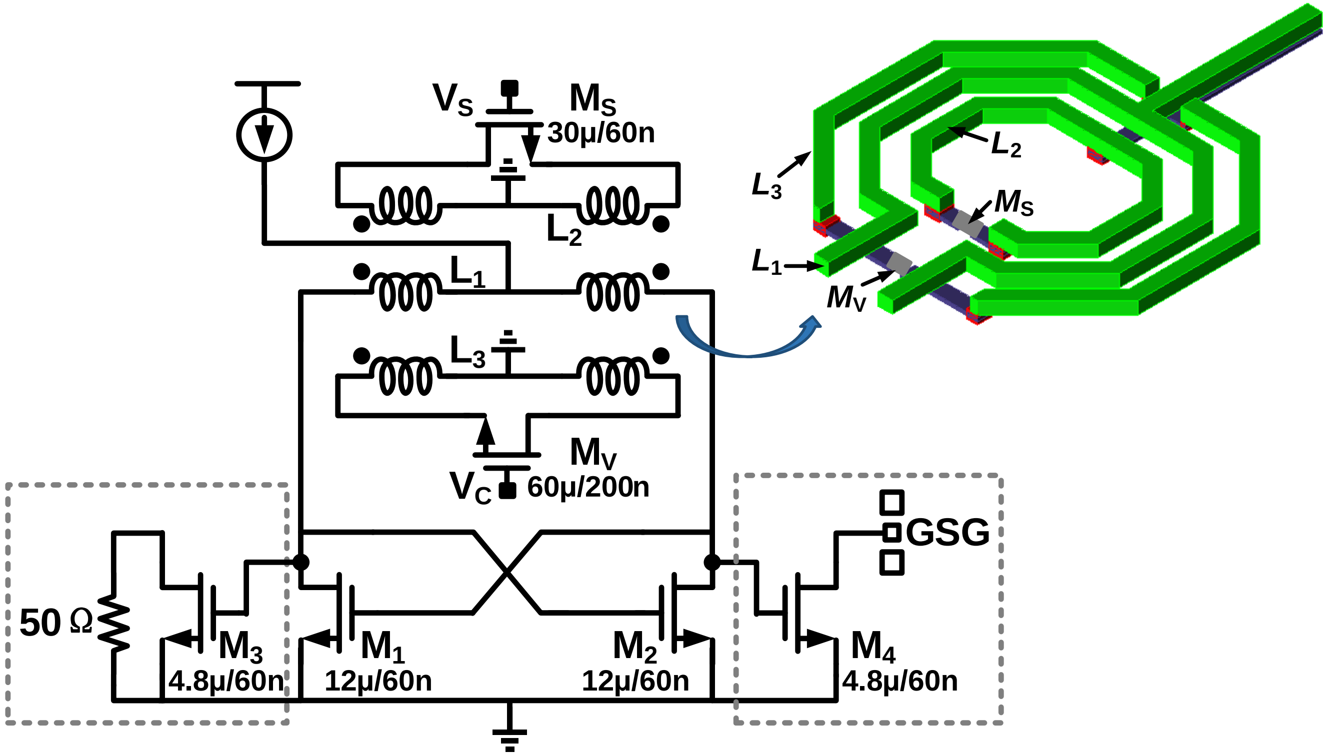
Layout of the Triple-Coil Tank

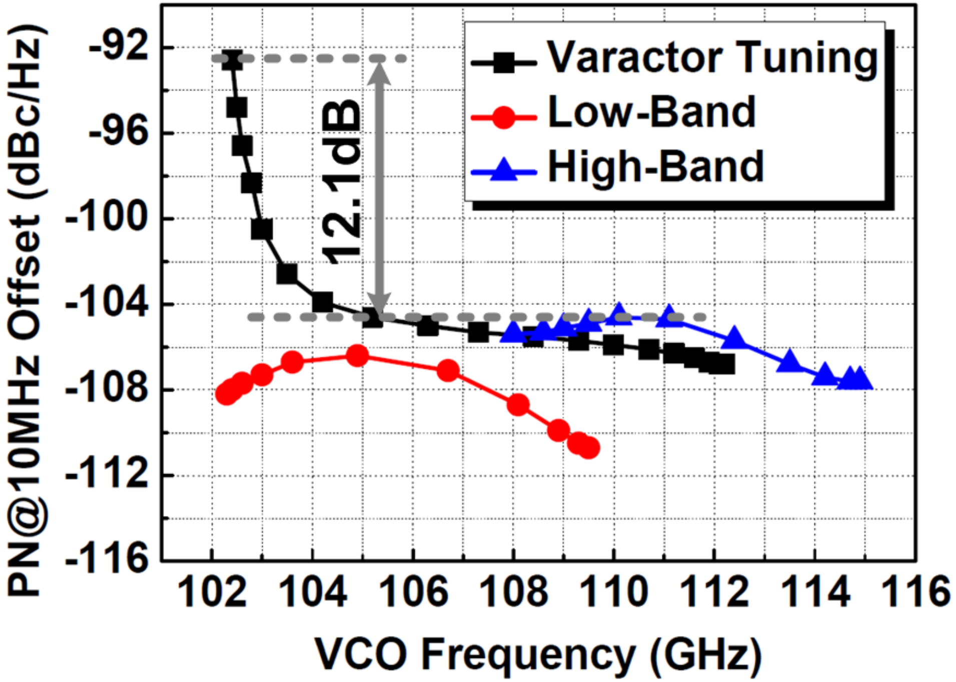


Simulated effective L_1 and tank Q

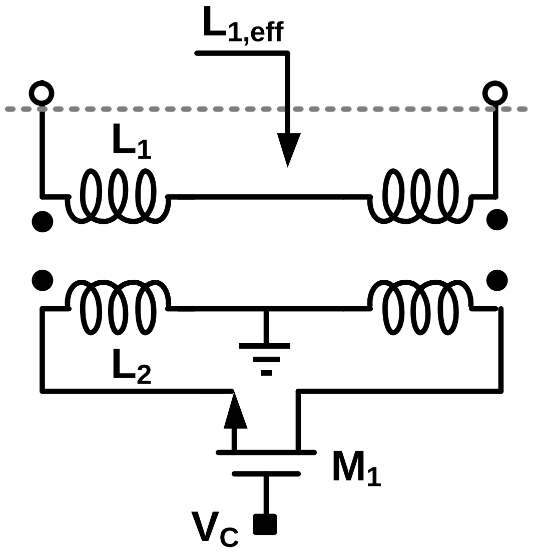
Proposed 110-GHz Varactor-Less Oscillator

- Two fundamental oscillators: one with magnetic tuning and another with varactors → The phase noise of the proposed magnetic-tuning design is improved up to 12 dB

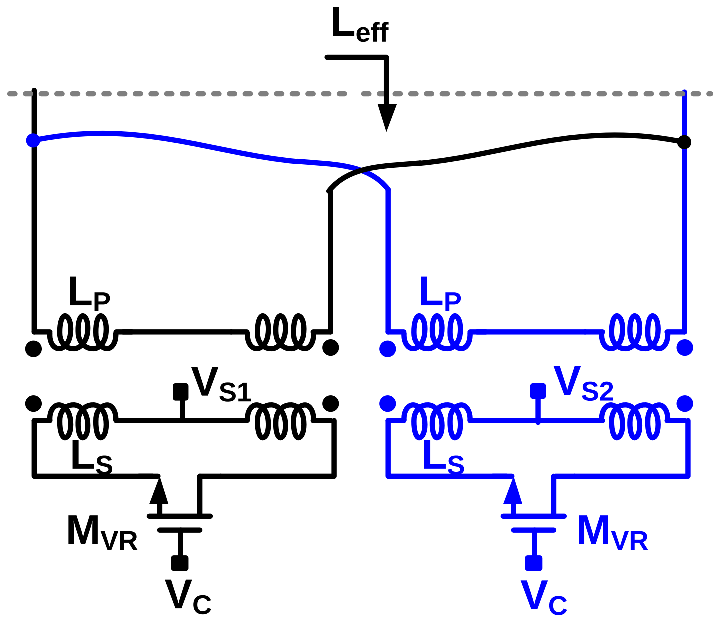




Linearized Technique for Sub-THz Oscillator

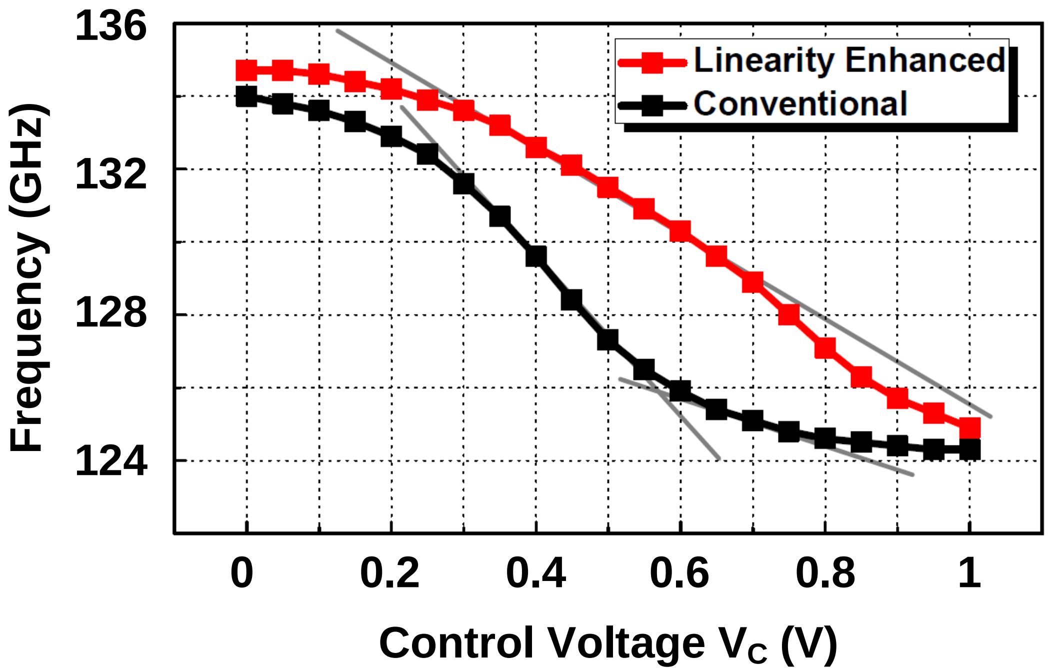


Conventional Variable Inductor



Proposed Linearity Enhanced Variable Inductor

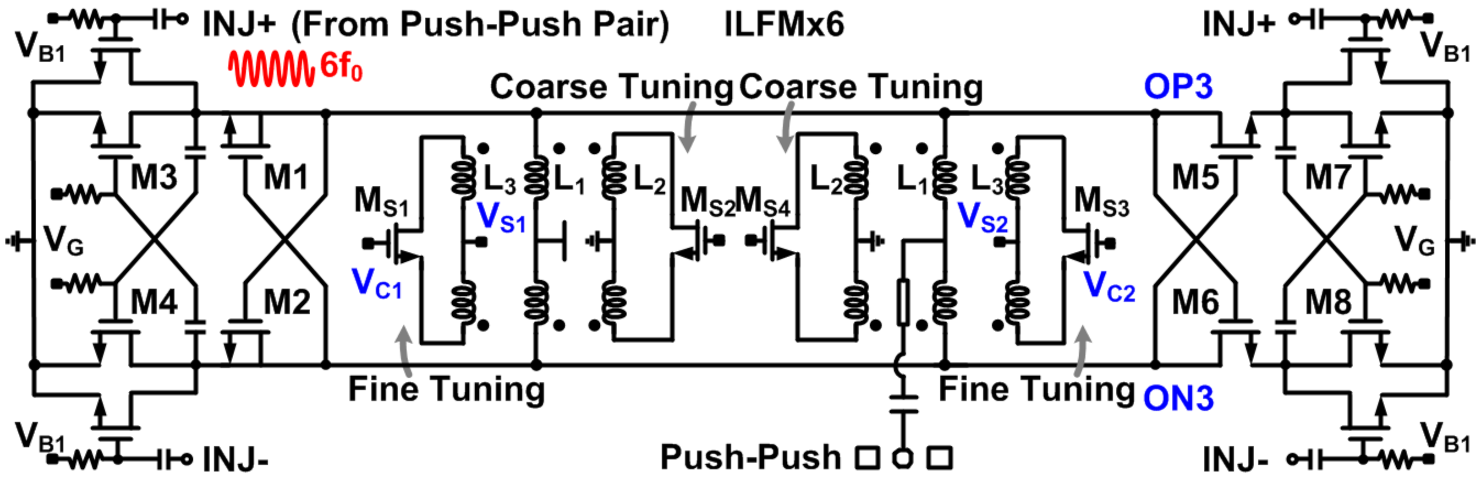
[X. Liu, JSSC'20]

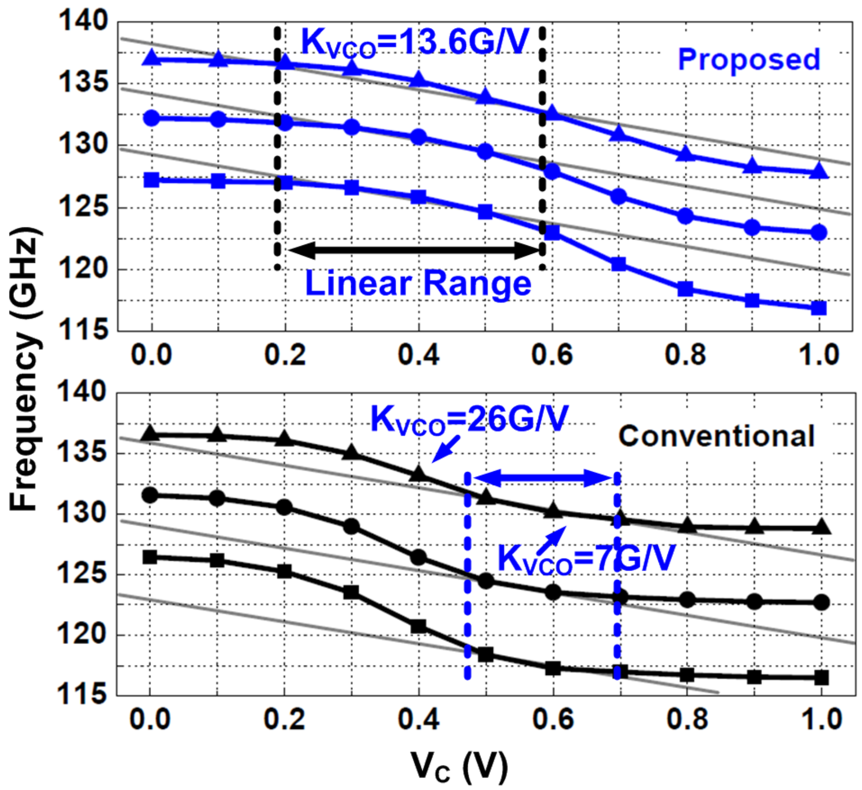


Simulated Frequency Tuning Curves of the VCOs Using Variable Inductors

- Variable resistor is not changed linearly → VCO gain varies significantly
- Distributed bias → Compensates the nonlinearity of the inductance changing

Proposed 140-GHz Varactor-Less Oscillator





Measured Frequency Tuning Range:
116.9-to-136.9 GHz

- Two identical oscillators coupled for distributed bias → Improve the linearity
- Conventional nonlinear oscillator → K_{VCO} varies by 3.7 times
- Proposed linear oscillator → K_{VCO} keeps almost constant in the linear range

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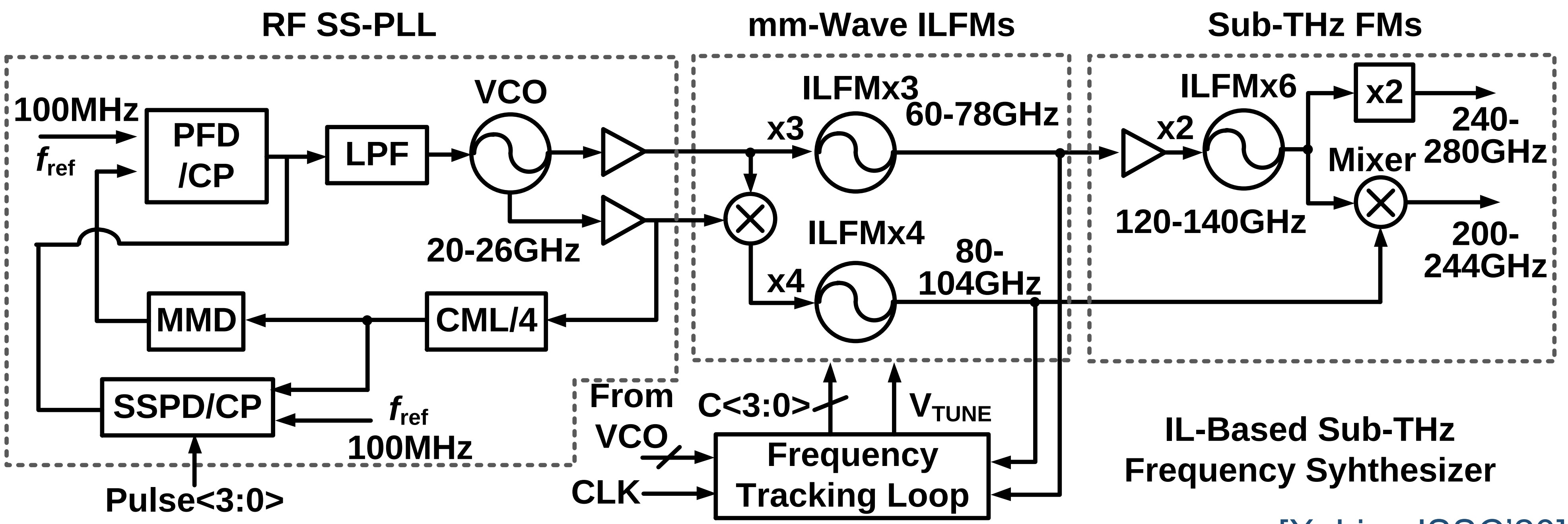
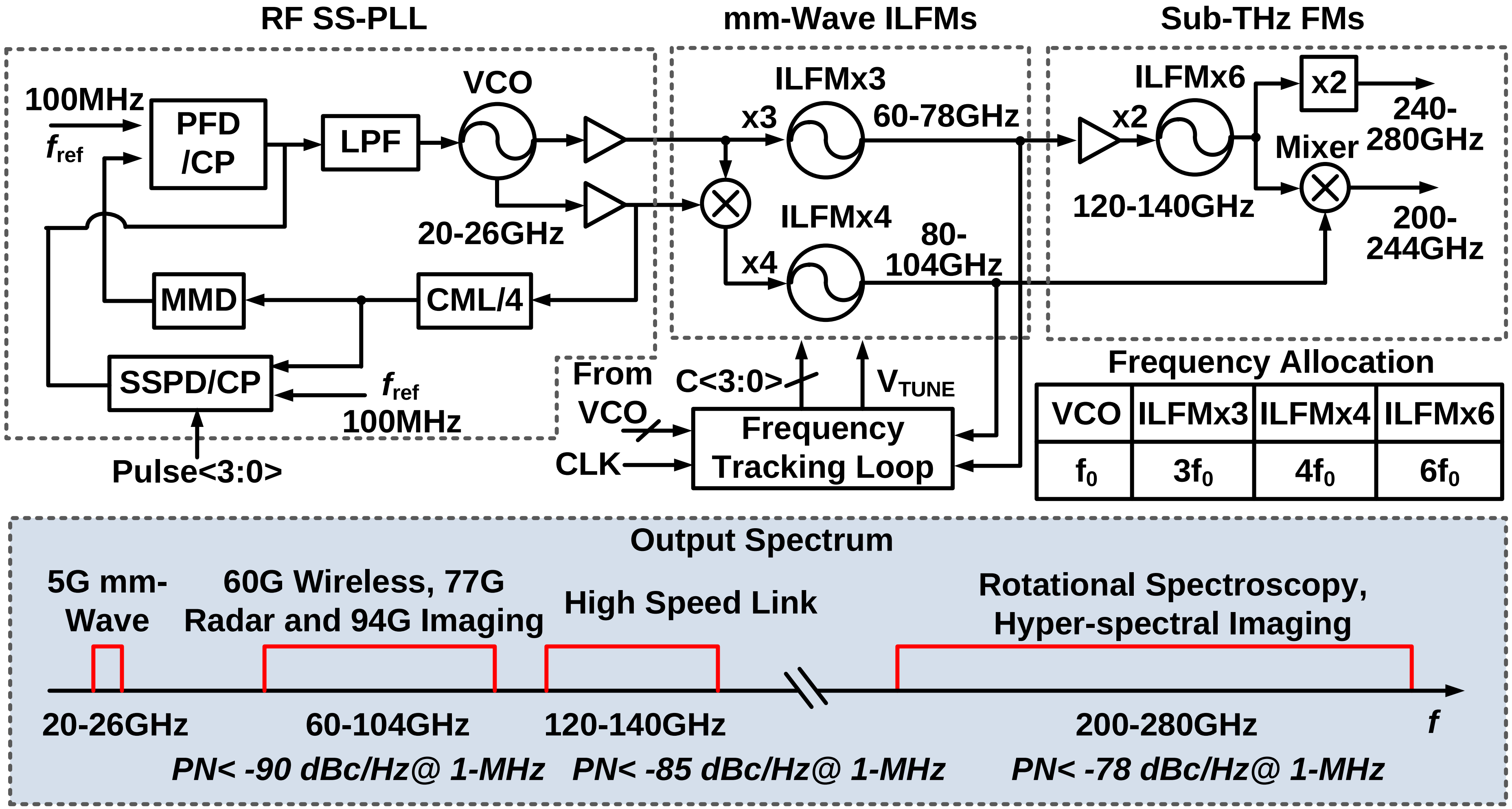
Mm-Wave/THz Signal Generation System



[X. Liu, JSSC'20]

- Sub-Sampling RF PLL → Low in-band phase noise
- Injection-Locked-based mm-Wave LO generation chain → Low phase noise
- Mixing-Based sub-THz frequency multipliers (FMs) → Frequency extension
- Frequency tracking loop → Automatic frequency and amplitude calibration

Frequency Plan

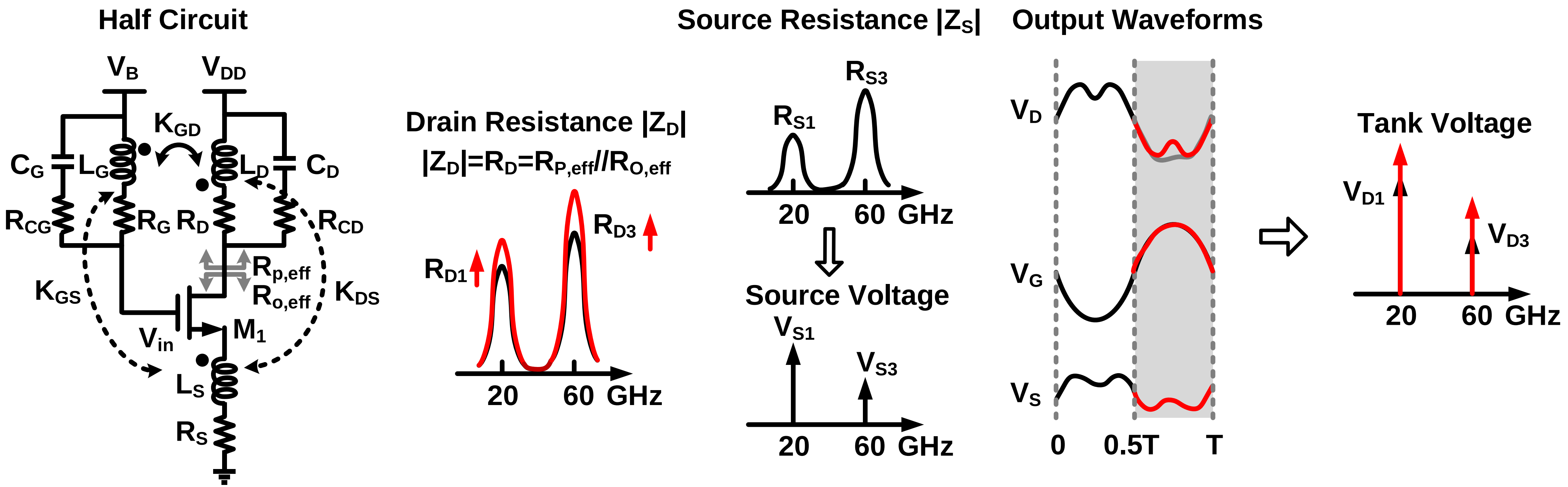


Frequency Allocation

VCO	ILFMx3	ILFMx4	ILFMx6
f_0	$3f_0$	$4f_0$	$6f_0$

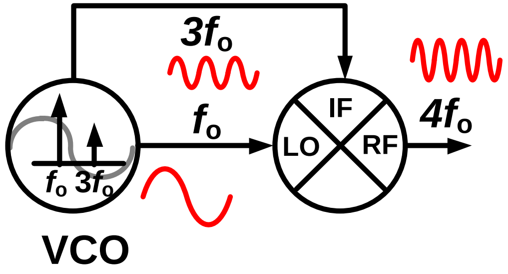
- The outputs are ready for various emerging applications

20-GHz VCO with Third-Harmonic Extraction



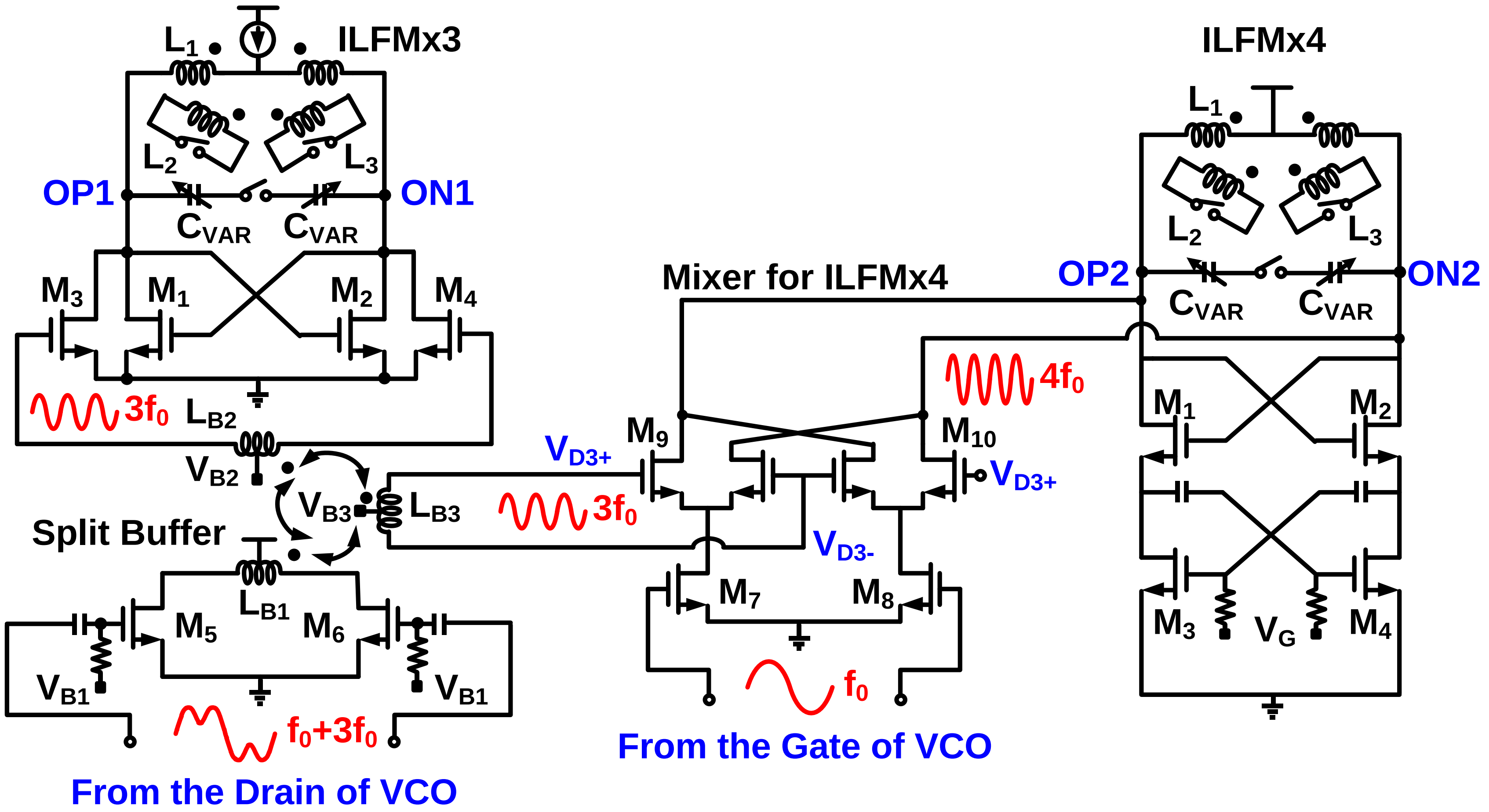
- Equivalent resistances R_{D1} and R_{D3} are significantly boosted
- The proposed harmonic extraction technique improves the third-harmonic output amplitude and phase noise of the VCO

ILFM-Based Mm-Wave LO generation Chain



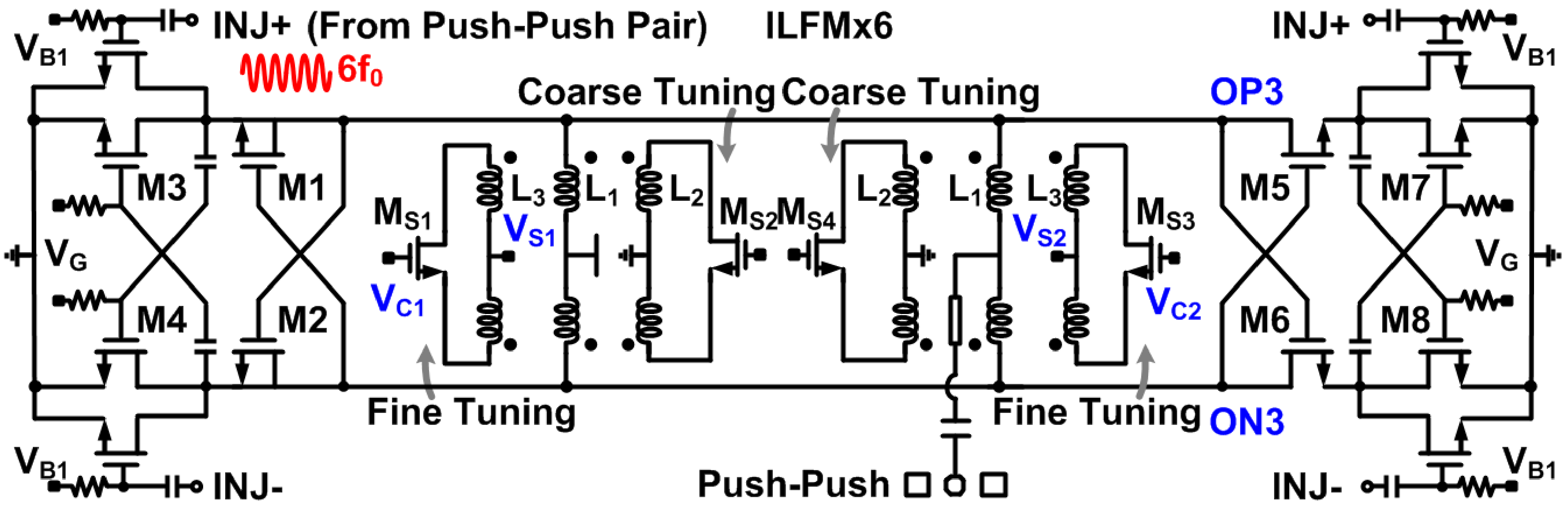
Frequency Allocation

VCO	ILFMx3	ILFMx4
f_0	$3f_0$	$4f_0$



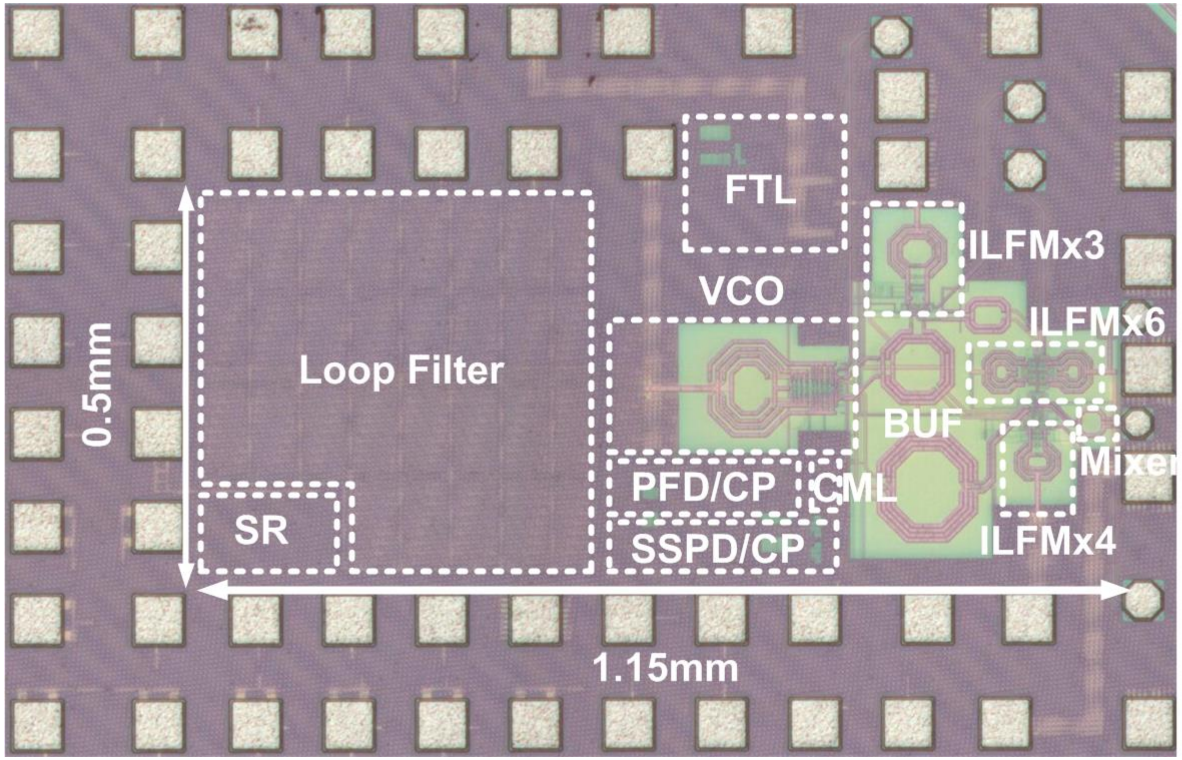
- Signals from the VCO are split into two paths for injection to ILFMx3 and ILFMx4
- Self-mixing the fundamental-harmonic and enhanced third-harmonic for fourth harmonic extraction→ Compact and high efficiency

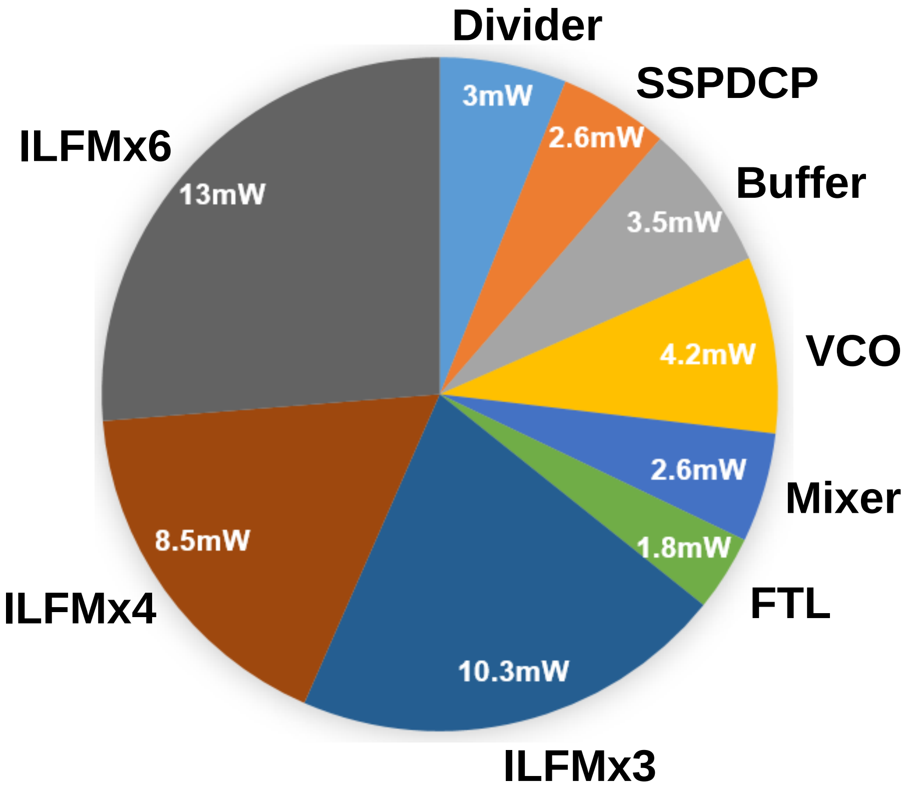
Sub-THz ILFMx6



- Two identical oscillators coupled for distributed bias → Improve the linearity
- Negative source degeneration cross-coupled pair for gm-boosting

Chip Photograph





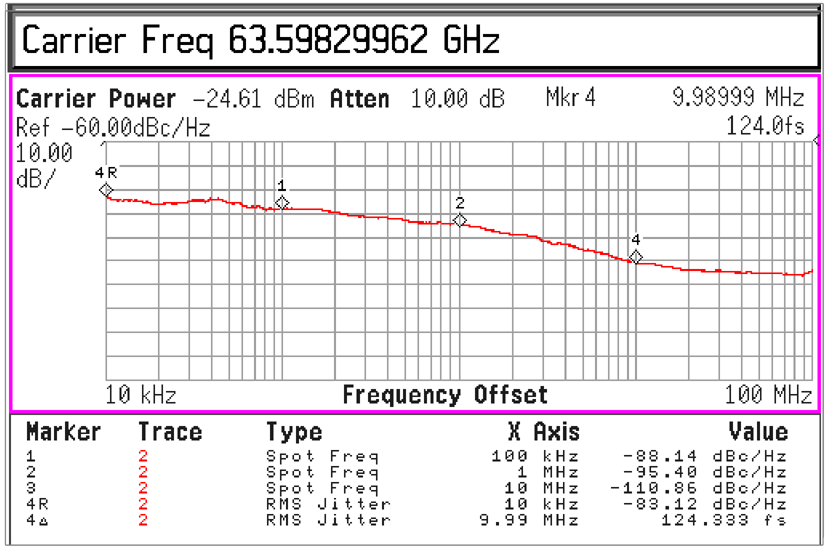
Fabricated in 65-nm CMOS

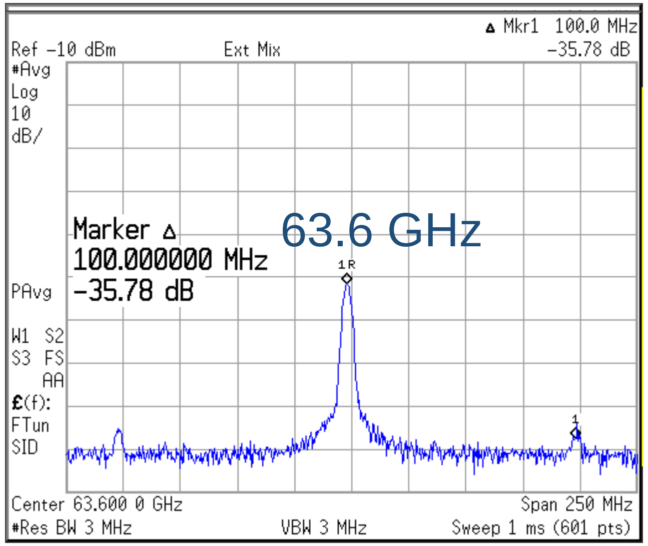
Core area: 0.58 mm^2

Total DC power consumption

49.5 mW

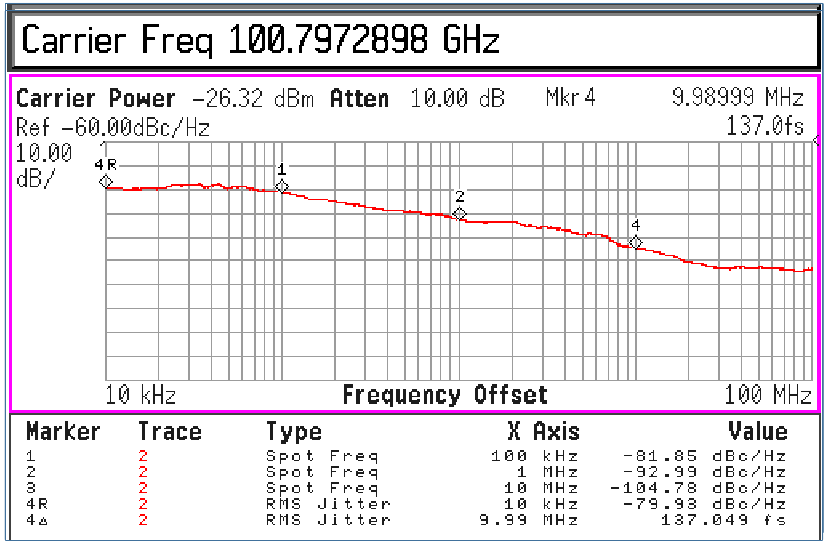
Measurement Results: ILFMx3 and ILFMx4

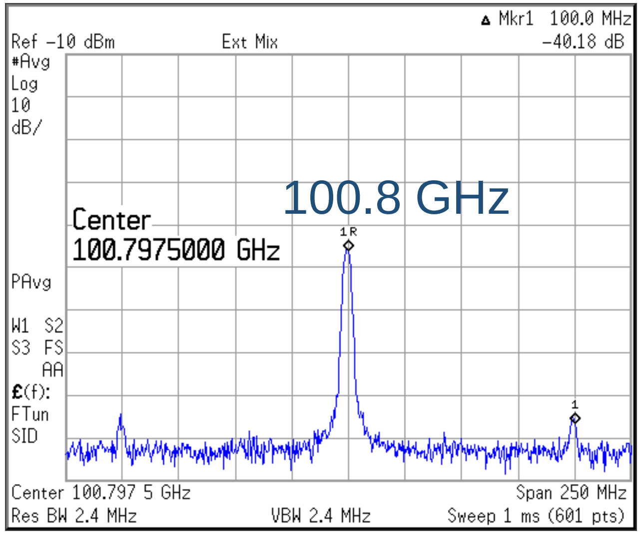




ILFMx3

- 63.6 GHz
- PN: -95.4 dBc/Hz@1M
- PN: -111 dBc/Hz@10M
- Jitter: 124 fs (10k-10M)

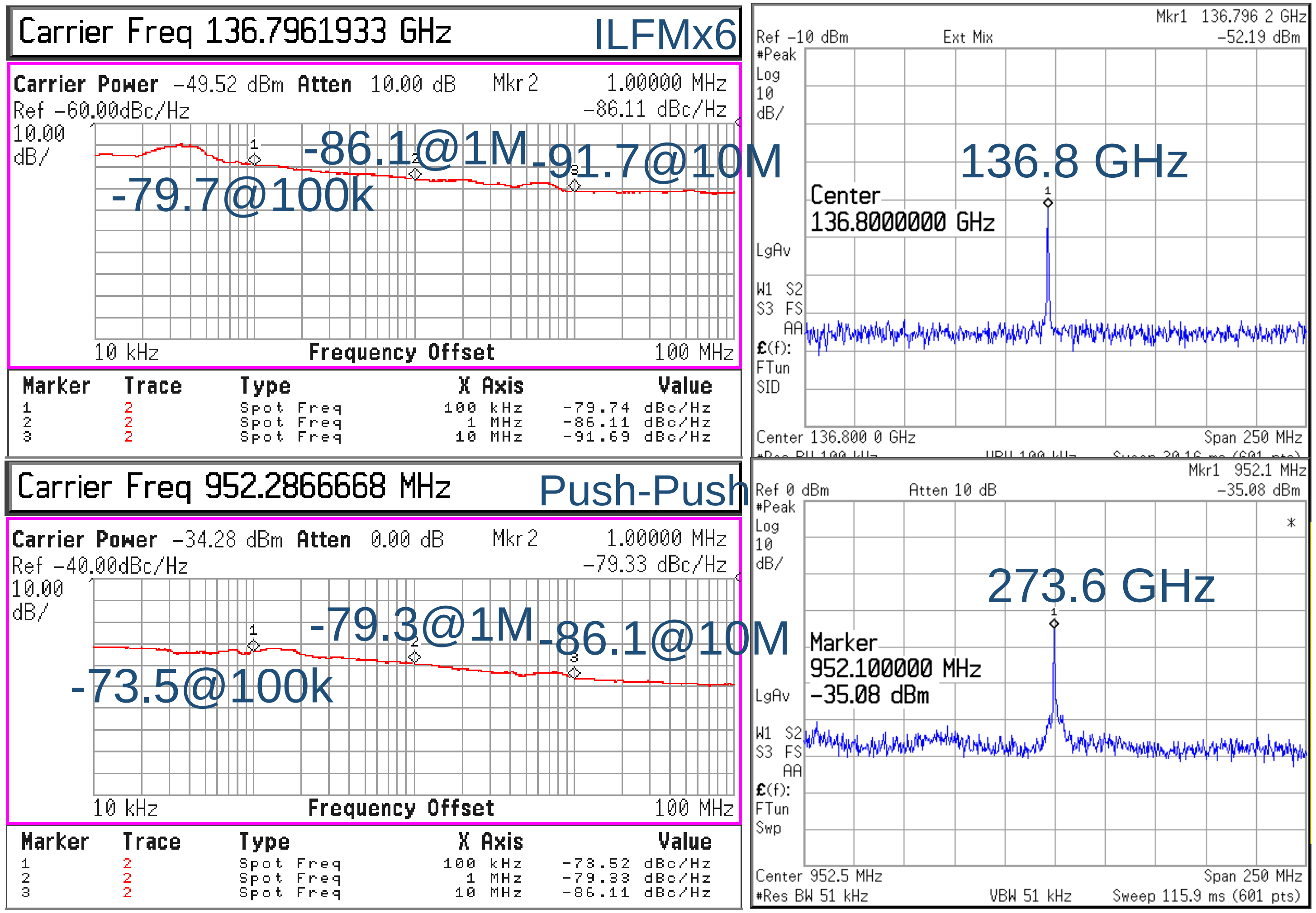




ILFMx4

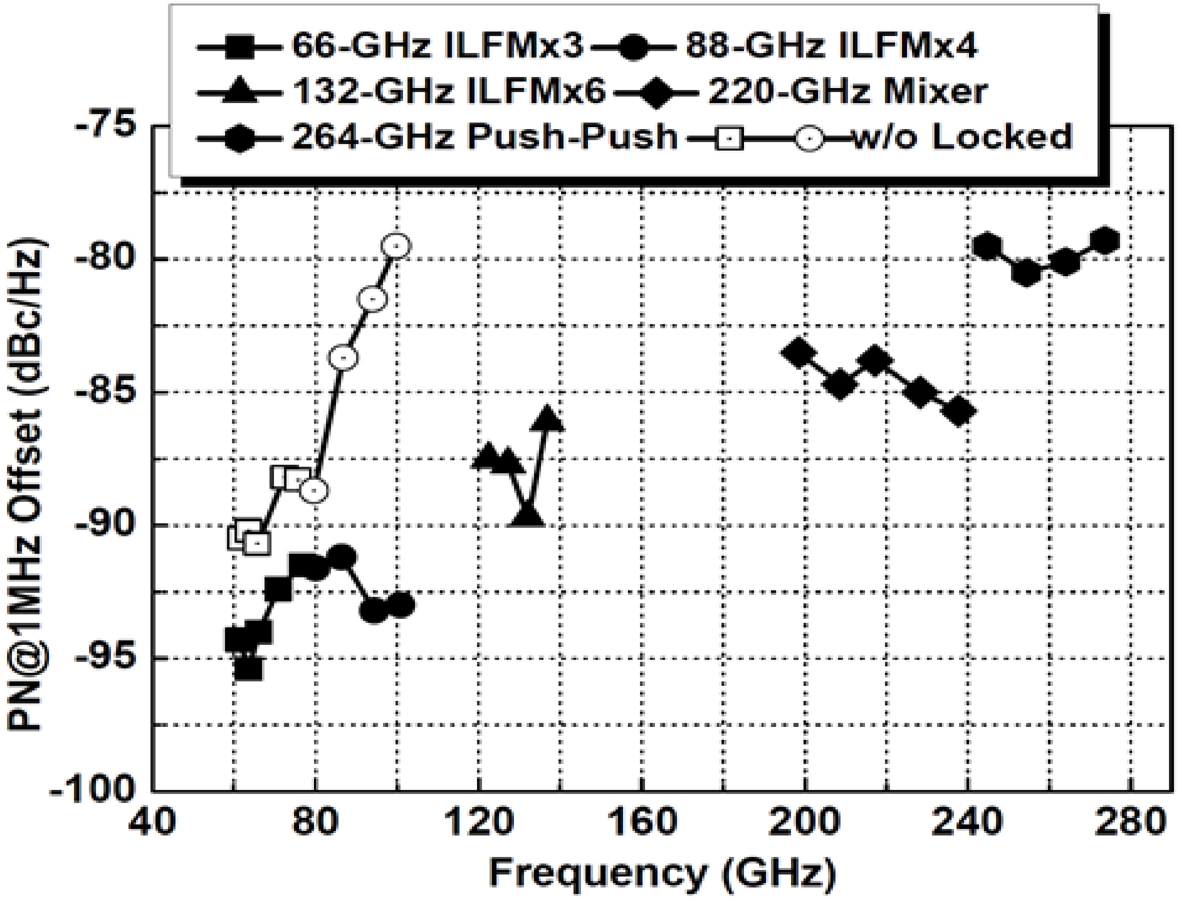
- 100.8 GHz
- PN: -93 dBc/Hz@1M
- PN: -104.8 dBc/Hz@10M
- Jitter: 137 fs (10k-10M)

Measured Results: ILFMx6 and Push-Push



Push-Push: 22.72x12+0.952=273.6 GHz, PN: -79.3 dBc/Hz@1M

Measured Phase Noise Across the Tuning Range



Measured Closed-Loop Phase Noise at 1-MHz Offset

From -79.3 dBc/Hz to -95.4 dBc/Hz

Performance Comparison: mm-Wave PLLs

	Y. Chao TMTT'15	V. Szortyka JSSC'15	T. Siriburanon JSSC'16	A. Hussein ISSCC'17	Z. Huang JSSC'19	Z. Zong JSSC'19	This Work JSSC'20	
Frequency (GHz)	96.8~108.5	53.8~63.3	55.6~65.2	50.2~66.5	82~107.6	57.6~67.2	61.2~100.8	122.4~136.8
Tuning Range	11.4%	16.2%	15.9%	28%	27%	15.6%	43.7%	11.1%
PLL Type	CPPLL	SSPLL	SSPLL	ADPLL	ADPLL	ADPLL	SSPLL	
Reference (MHz)	200	40	40	100	125	100	100	
PN@100K (dBc/Hz)	-84	-89/-92	-78.5	-78.8/-82.7	-84.2/-87.1	-81/-84	-80/-83.1	-72.6/-75
PN@1M (dBc/Hz)	-88	-88~-92	-92	-88 /-94.5	-79 / -82	-89/-92	**-90.1/-95.4**	**-86.1/-89.7**
PN@10M (dBc/Hz)	-104	-108	-122	-116/-122.5	-104/-110	-118.4	-103/-110.9	-91.7/-94*
DC Power (mW)	14.1	42	32	46	35.5	41.5	23.6	36.6
Spur (dBc)	-41	-40	-73	-48.3/-52.2	-34/-52	-65	-35.7/-48.7	< -33
Jitter (ps)	N/A	0.2/0.35	0.29	0.223/0.302	0.276/0.328	0.213/0.241	**0.124 / 0.155**	**0.159**
FoM_J (dB)	N/A	-237.7	-235.7	-236.4	-235.7	-237.2	**-244.4/-242.5**	**-240.3**
FoM (dBc/Hz)@1M	-177	-171.8	-172.6	-172.3	-164.8	-171	**-177.7**	**-176.1**
FoM_T(dBc/Hz)@1M	-178.1	-176	-176.6	-181.3	-173.4	-174.9	**-190.5**	-177
Process (CMOS)	65nm	40nm	65nm	65nm	65nm	28 nm	65nm	
Area (mm^2)	0.39	0.16**	1.08***	0.45	0.36	0.38	0.58	

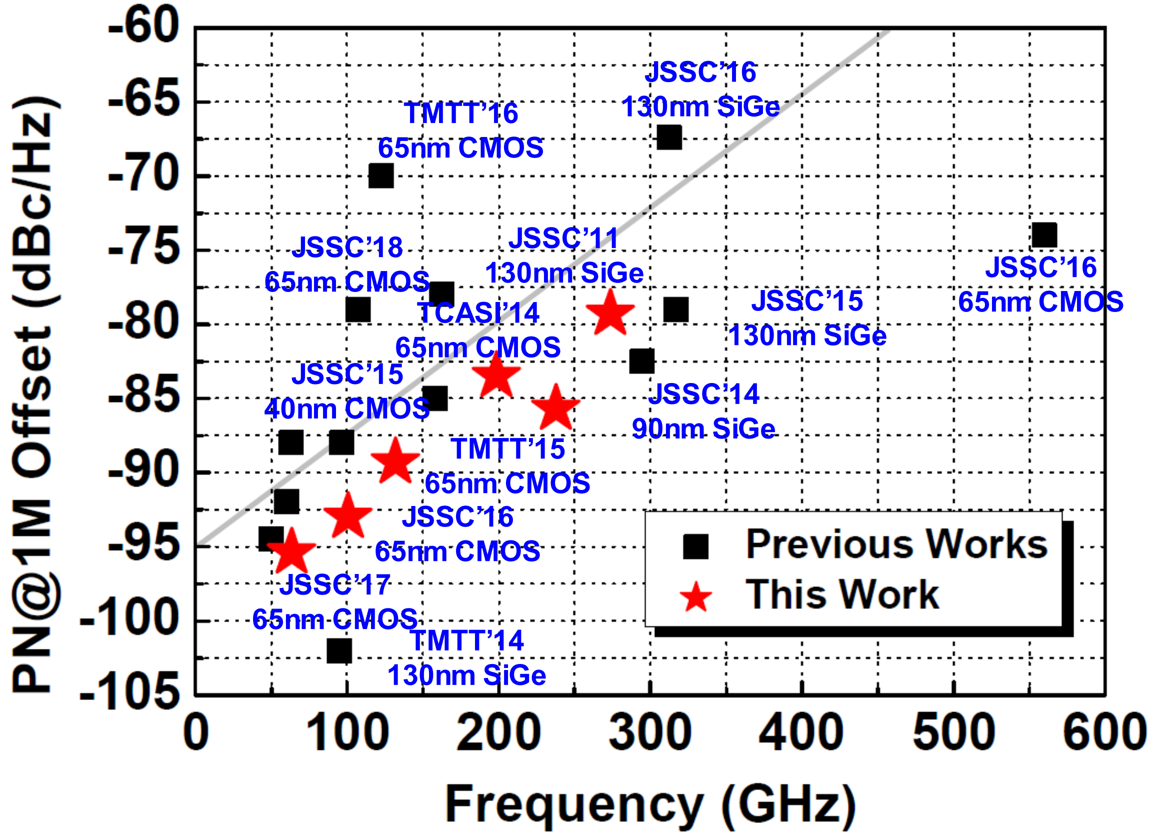
*Flatten by the high noise floor, **With Pads, *** Off-chip LPF, FoM_J=20log(jitter/1s)+10log(Pdc/1mW), FoM=PN(f0)-20log(f/f0)+10log(Pdc/1mW), FoM_T=FoM_2+20log(TR/10%)

Performance Comparison: THz Signal Generators

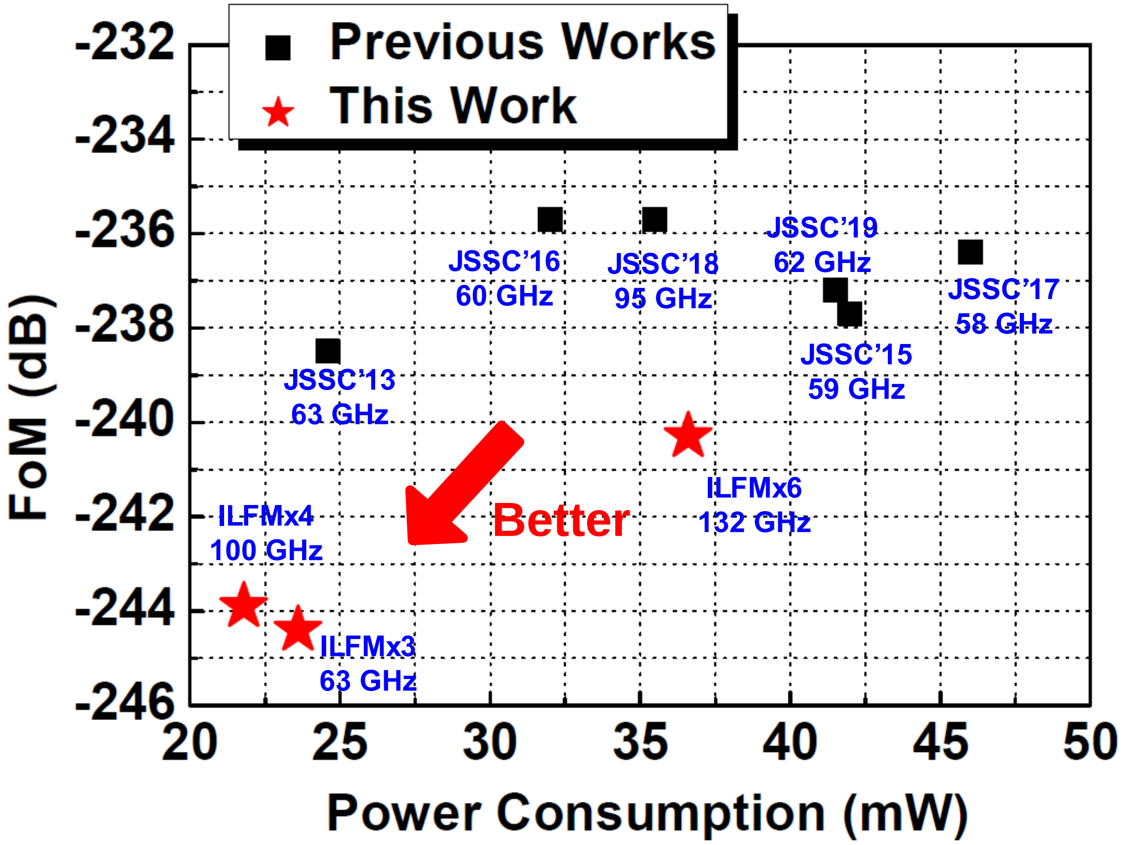
	P. Chiang JSSC'14	N. Sharma VLSI'16	Y. Zhao JSSC'16	C. Wang JSSC'17	C. Jiang TMTT'19	This Work JSSC'20
Frequency (GHz)	291.5	231.5	549.5	270	317	236
Tuning Range (GHz)	280-to-303	208-to-255	539-to-560	220-to-320	302-to-332	198-to-274
Bandwidth (GHz)	23	47	21	100	30	76
Type	PLL	PLL	SSPLL	Free running	Freq. stabilized	SSPLL
Reference (MHz)	95	125	108	N/A	N/A	100
PN@100K (dBc/Hz)	-77.8	N/A	-71	N/A	-72.4	**-78.2**
PN@1M (dBc/Hz)	-82.5	-80	-74	-102*	-78.5	**-85.7**
PN@10M (dBc/Hz)	-89.6	N/A	-85	N/A	-96.7	**-104.7**
DC Power (mW)	376	1400	172	1700	51.7	**49.5**
Psat (dBm)	-14	-11	-27	-2.8	-13.9	-11
DC-to-RF Efficiency	0.011%	0.006%	0.001%	0.031%	0.079%	**0.16%**
Process	90nm SiGe	65nm CMOS	65nm CMOS	65nm CMOS	130nm SiGe	65nm CMOS
Area (mm^2)	2.56	5.6	2.79	6	0.85	0.58

***External signal generator rather than on-chip VCOs**

Performance Comparison with State-of-the-Art



Phase Noise at 1-MHz Offset



FoM=20log(jitter/1s)+10log(Pdc/1mW)

Conclusion

- Magnetic tuning is proposed to improve the tuning range and phase noise of the mm-Wave and THz fundamental oscillators
- Multi-band magnetic tuning and distributed bias techniques to improve the tank Q and linearity of the sub-THz oscillators
- Enhanced harmonic extraction and self-mixing-based method for frequency multiplications by three and four
- Design and integration of a whole PLL-based signal generation system, which can generate accurate, high purity signals from 61.2-to-100.8 GHz, 122.4-to-136.8 GHz and 198.5-to-273.6 GHz

Thank You!

Reference

1. **Xiaolong Liu**, Yue Chao and Howard C. Luong, "A 59-to-276-GHz CMOS Signal Generator Using Varactor-Less VCO and Dual-Mode ILFD," *IEEE Journal Solid-State Circuits(**JSSC**)*, vol 56 no 8 pp 2324 2334 Aug 2021.
2. **Xiaolong Liu** and Howard C. Luong, "A Fully Integrated 0.27-THz Injection-Locked Frequency Synthesizer with Frequency-Tracking Loop in 65-nm CMOS," *IEEE Journal Solid-State Circuits (**JSSC**)*, vol. 55, no. 4, pp. 1051–1063, April 2020.

Thank You!