Low-phase-noise Millimeter-wave Fundamental CMOS Oscillators: from Multi-core to Many-core

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Workshop on IC Advances in China (ICAC)

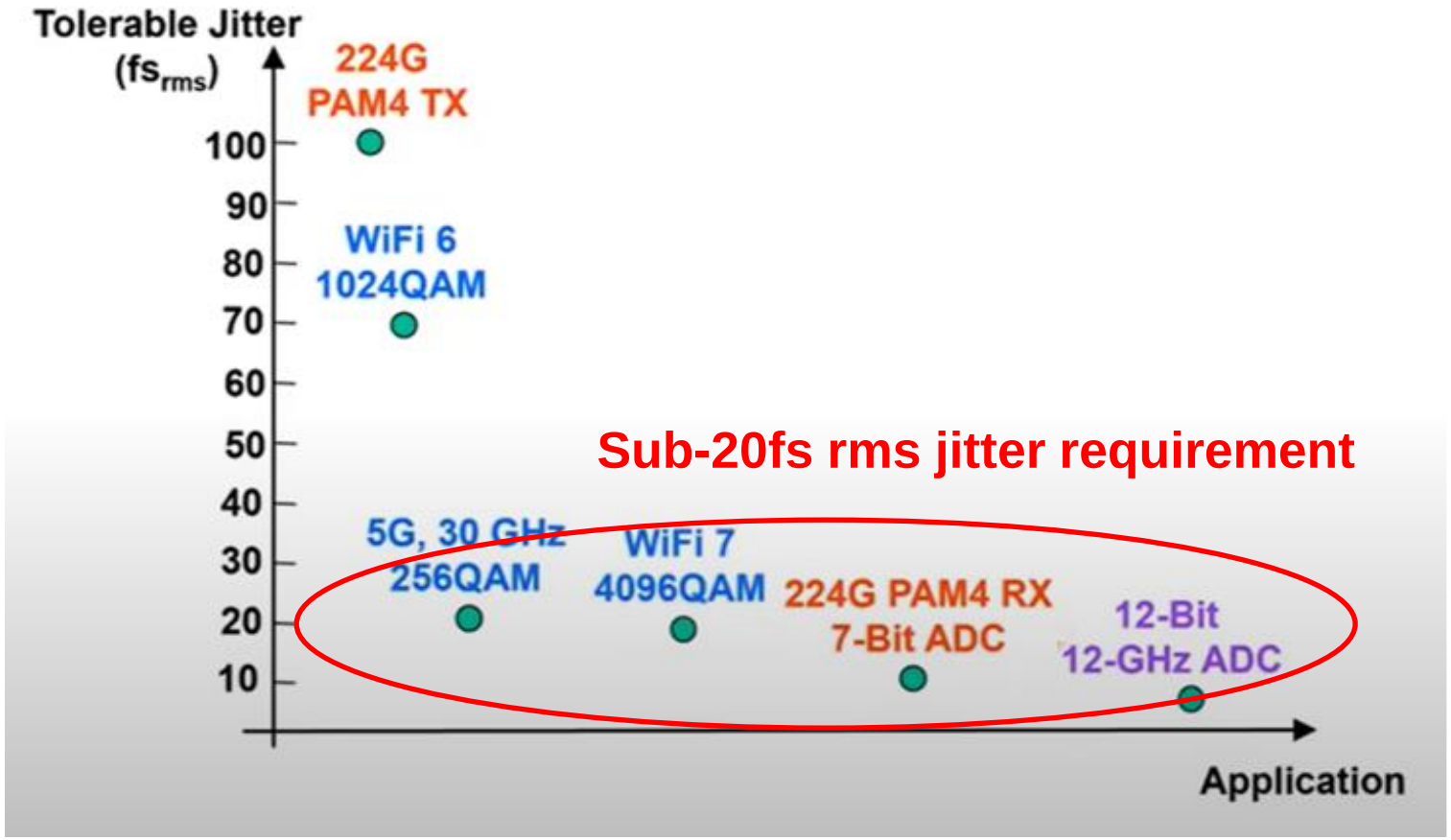
华人芯片设计技术研讨会2022

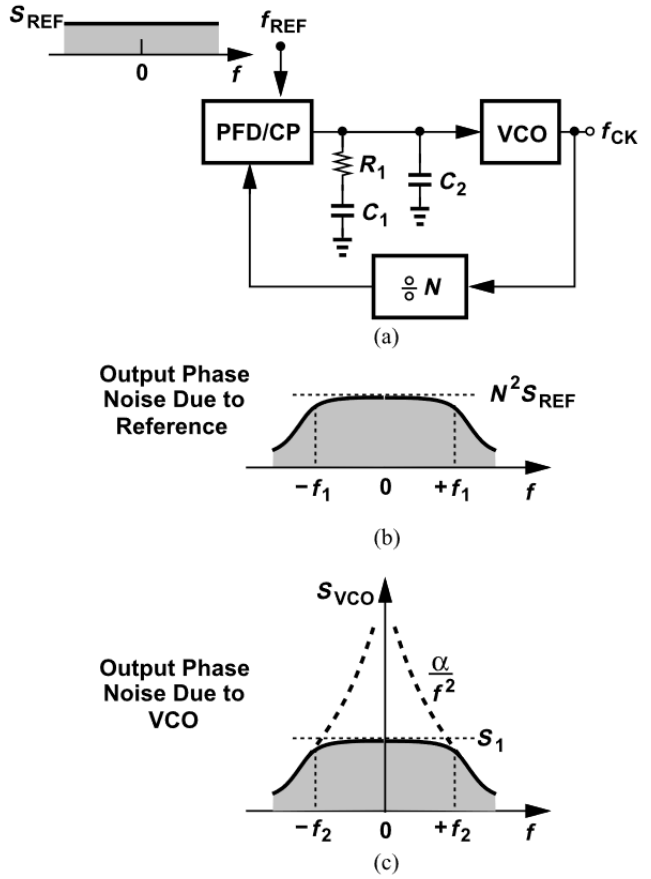
Outline

- Introduction
- Challenges for mm-Wave High-Quality VCOs
- From Multi-Core to Many-Core
  - Synchronization Methods
  - Core Floorplan
- Mesh-Topology 16-Core Oscillator Prototype
  - Implementation Details
  - Measured Results
- Conclusions

Requirement for High-Performance mm-Wave VCO

- **High-quality clock essential for varies applications** [Razavi, TCAS-I, 21]
  - **Sub-20fs rms jitter, VCO is one of the two main jitter contributors**





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The Phase Noise in mm-Wave VCOs

- **Leeson's equation**

$$L(\Delta\omega) \propto 10\log_{10}\left[\frac{K_B T R_P}{A^2 Q^2}\frac{\omega^2}{(\Delta\omega)^2}\right]$$

[D. B. Leeson, Proc. IEEE'66]

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[D. B. Leeson, Proc. IEEE'66]

- **A↑: Amplitude limited by process, reliability issue**
  - **Swing goes beyond supply voltage by techniques such as V_{GS} boosting.**
  - **Limited by process and reliability issue eventually.**

The Phase Noise in mm-Wave VCOs

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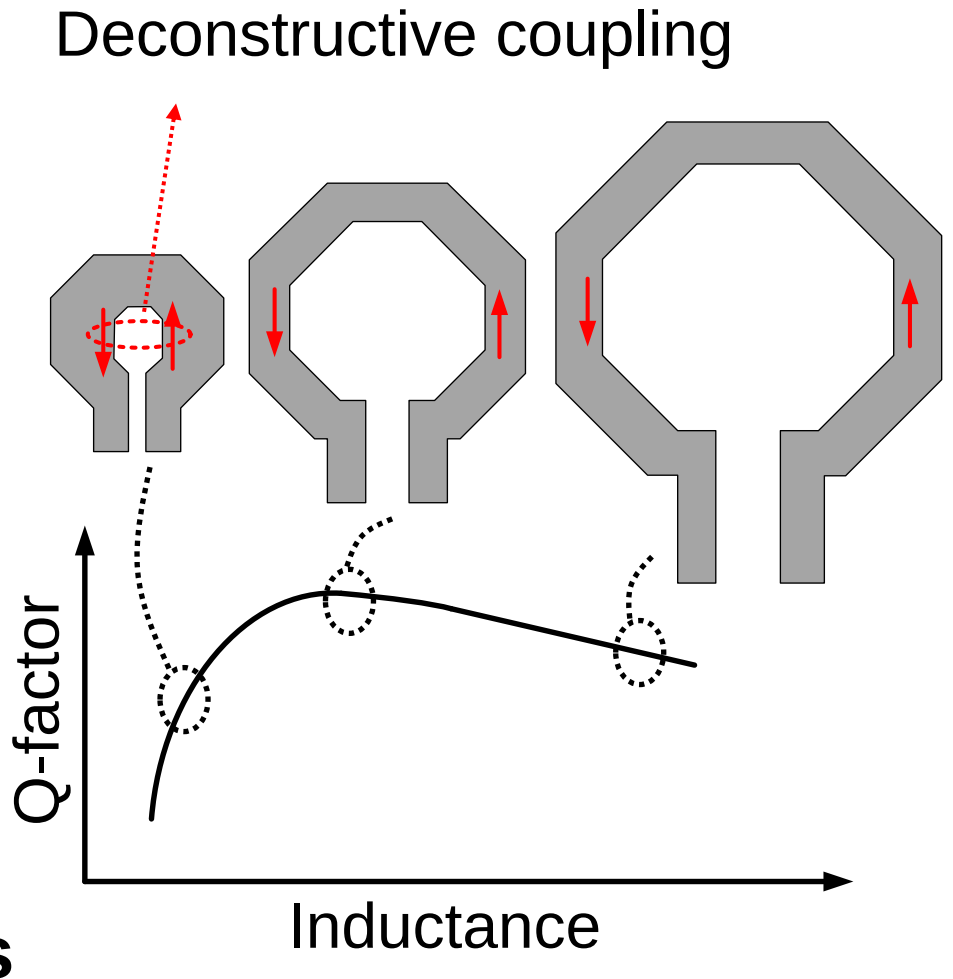
[D. B. Leeson, Proc. IEEE'66]

- **A↑: Amplitude limited by process**
- **Q↑: The mm-wave small inductance's Q problem**

The Degraded Q of Small Inductance

- **Small L desired for mm-wave VCOs**
  - Small inductance budget
  - Decent frequency tuning range
- **Inner edge deconstructive coupling degrades Q of small inductor**
- **PN in mm-wave VCO bounded by smallest realizable L with high Q**
- **Improved by circular-topology inductors**



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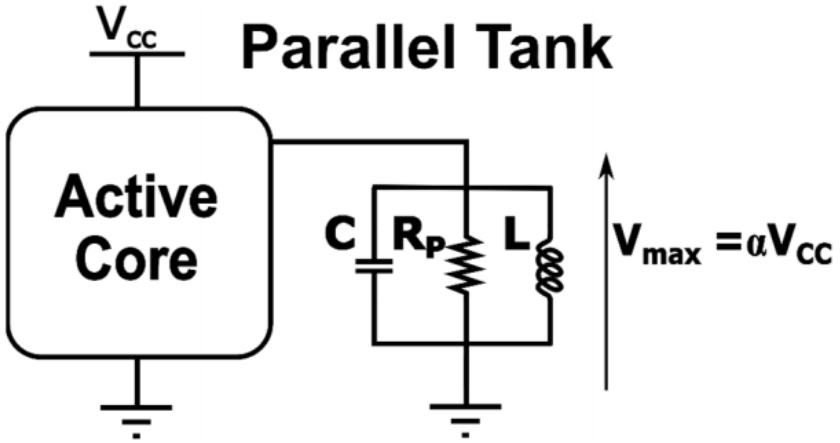
[D. B. Leeson, Proc. IEEE'66]

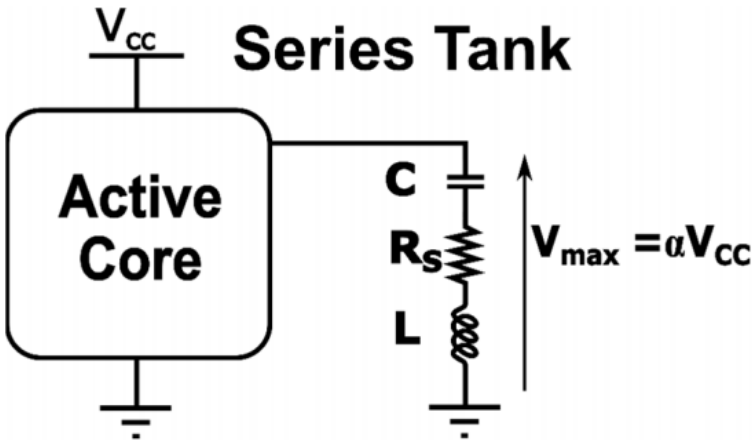
- $A\uparrow$: **Amplitude limited by supply voltage**
- $Q\uparrow$: **Tank Q limited by "Q of small inductance" problem**
- $R_P\downarrow$: **Need large power for same A, power-performance tradeoff**
  - **How to achieve small Rp?**

The First "Small R_P" Approach

- **The Series-Resonance VCO**

[A. Franceschin, ISSCC'22]





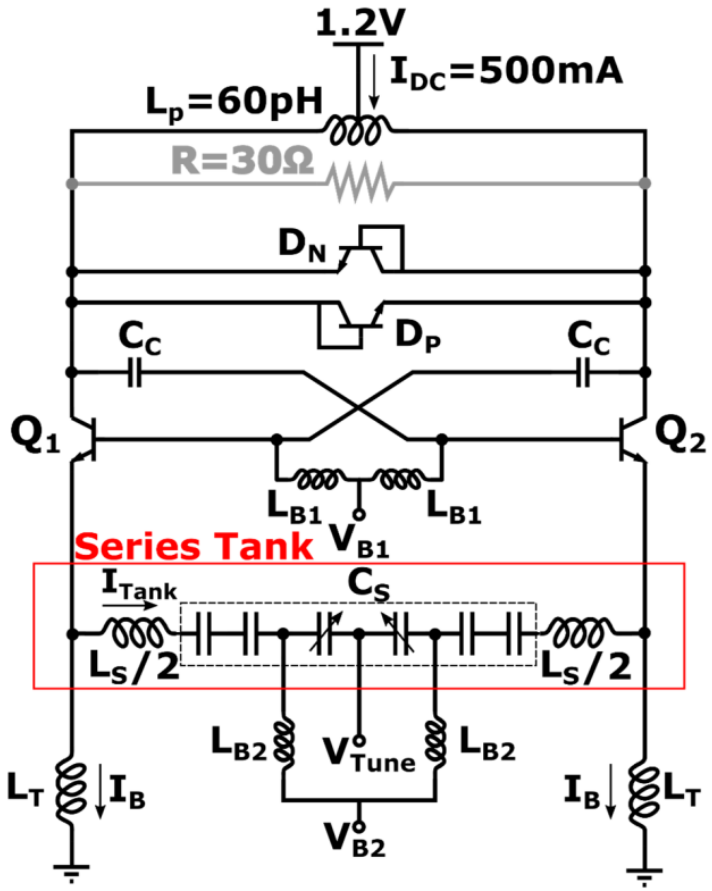
- **Parallel tank** oscillator: $P_{parallel} = \frac{V_{max}^2}{2R_P} = \frac{V_{max}^2}{2\omega_0 LQ}$
- **Series tank** oscillator: $P_{series} = \frac{V_{max}^2}{2R_s} = \frac{QV_{max}^2}{2\omega_0 L} = Q^2 P_{parallel}$

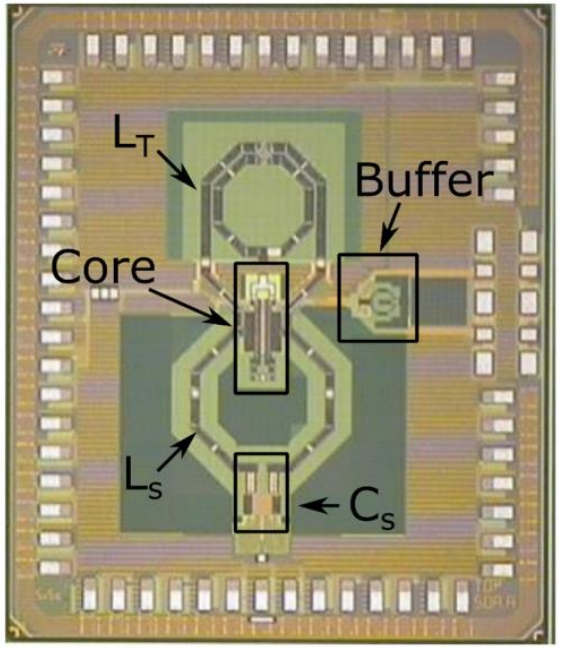
$$\mathcal{L}_{series} = \mathcal{L}_{parallel} - 10\log Q^2$$

The First "Small R_P" Approach

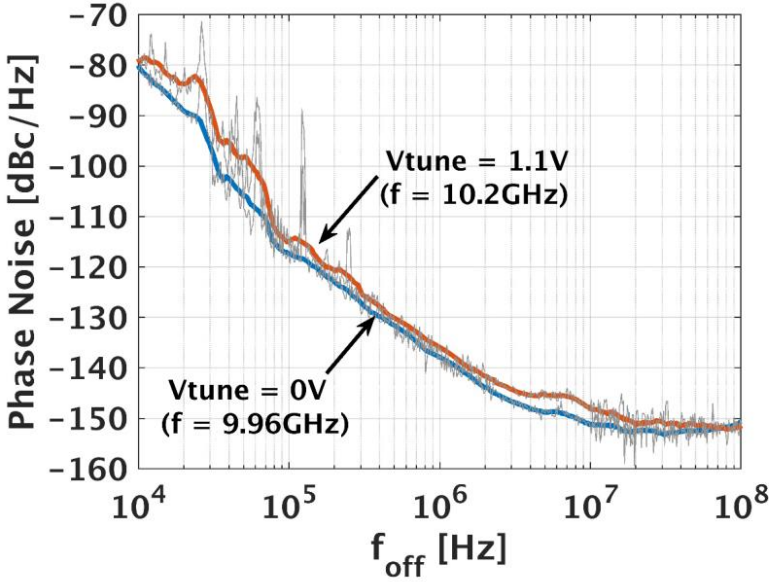
- **The Series-Resonance VCO**

[A. Franceschin, ISSCC'22]





- STMicro 55nm BiCMOS
- P_{DC} = 0.6W from V_{CC} = 1.2V



- Best PN @ 9.96 GHz: -138 dBc/Hz @1MHz
- Worst PN @ 10.2 GHz: -135.5 dBc/Hz @1MHz

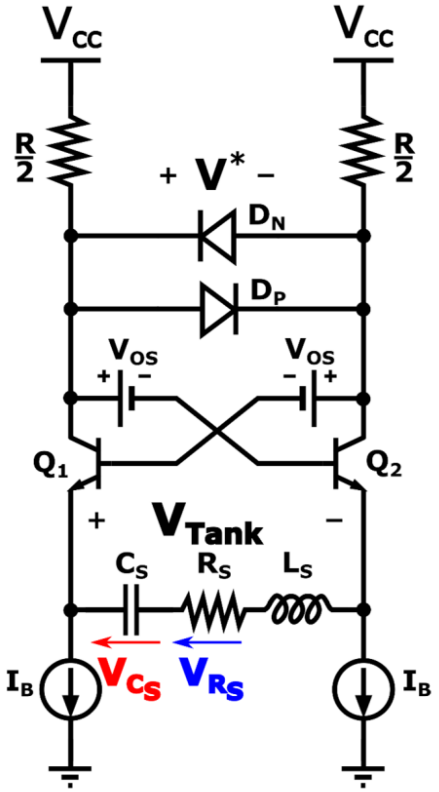
Phase noise at least 10dB below what reported so far in silicon

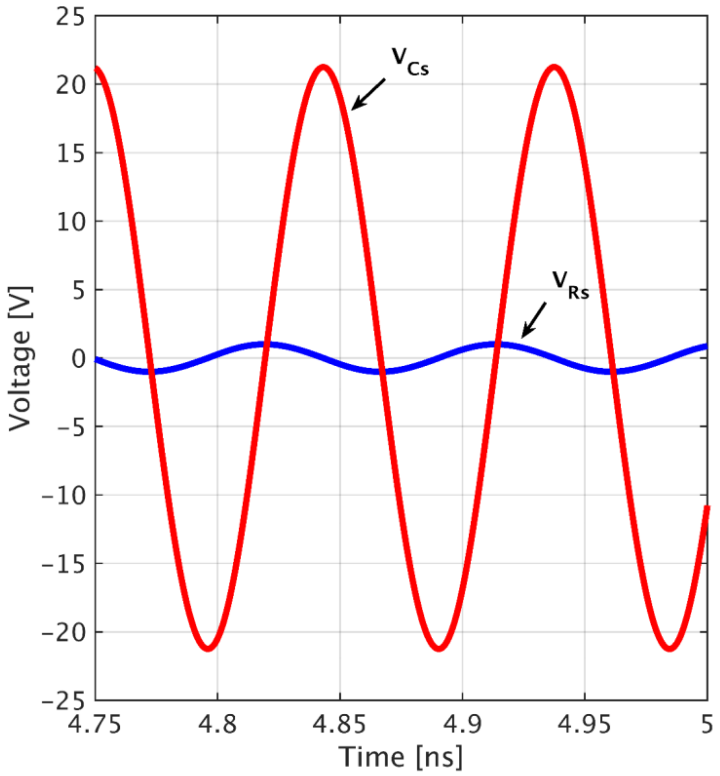
The First "Small R_P" Approach

- **The Series-Resonance VCO**

[A. Franceschin, ISSCC'22]

- **Main limitations:**
  - **Tuning Range: ~9%**
  - **Reliability: over-stressed**
  - **Challenge in CMOS**
  - **Not yet proven in mm-wave**





The Second "Small R_P" Approach

- **Multi-Core VCO**

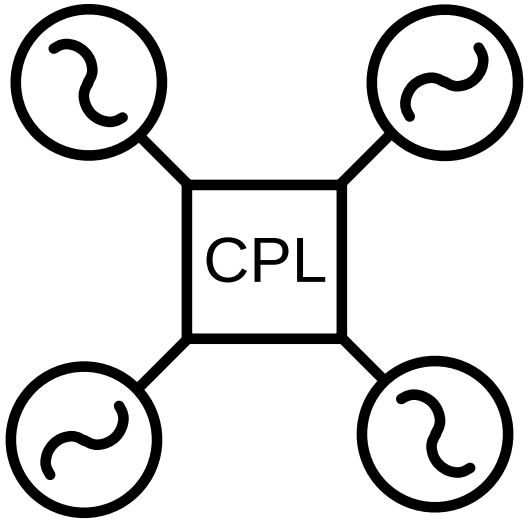
☺ **1/N times smaller R_P**

☺ **PN improved by 10log(N)**

☺ **Larger L in each core**

☹ **Large chip area**

→ **not significant in mm-wave**

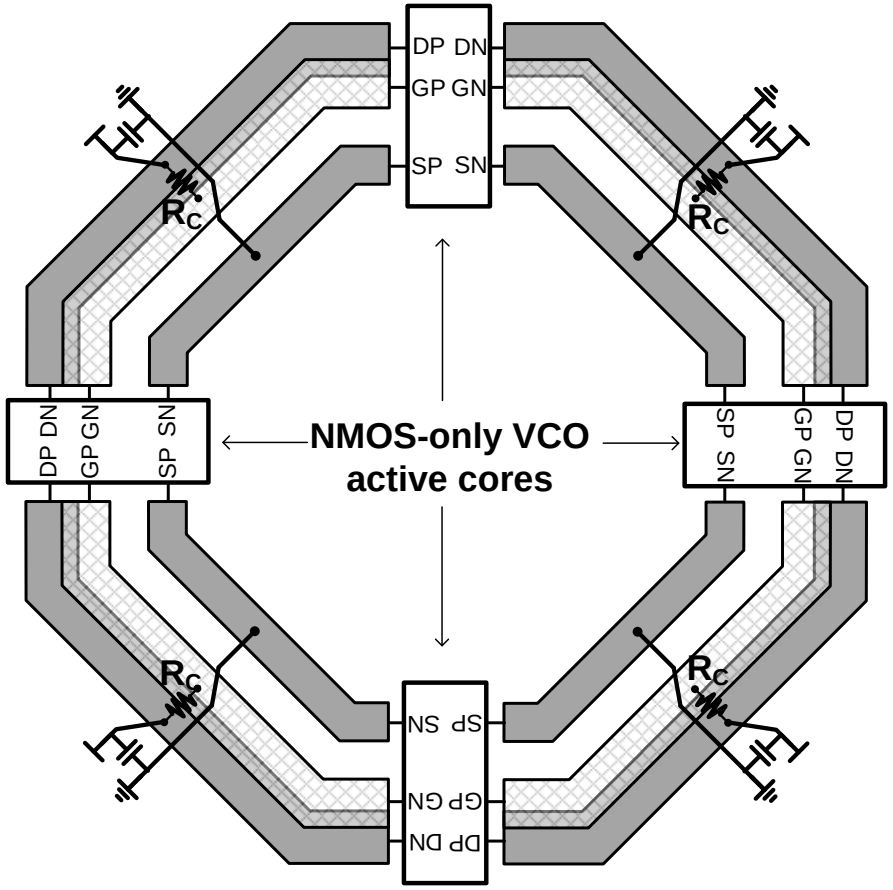


[F. Padovan, ISSCC'18]
[D. Murphy, JSSC'18]
[Y. Shu ISSCC'20]

*N: number of cores

The Second "Small R_P" Approach

- **A mm-Wave Quad-Core VCO example**



[H. Jia, ISSCC'21]

- **52.4~60.4GHz in 65nm CMOS**
- **-104.7dBc/Hz@1MHz from 59.1GHz**
- **186.5dBc/Hz FoM**

☺ **Slab high-Q small inductors**

☺ **Transformer enables NMOS-only VCO**

☹ **Complex route, difficult to extend to core number >4**

further PN improvement → from multi-core to many-core

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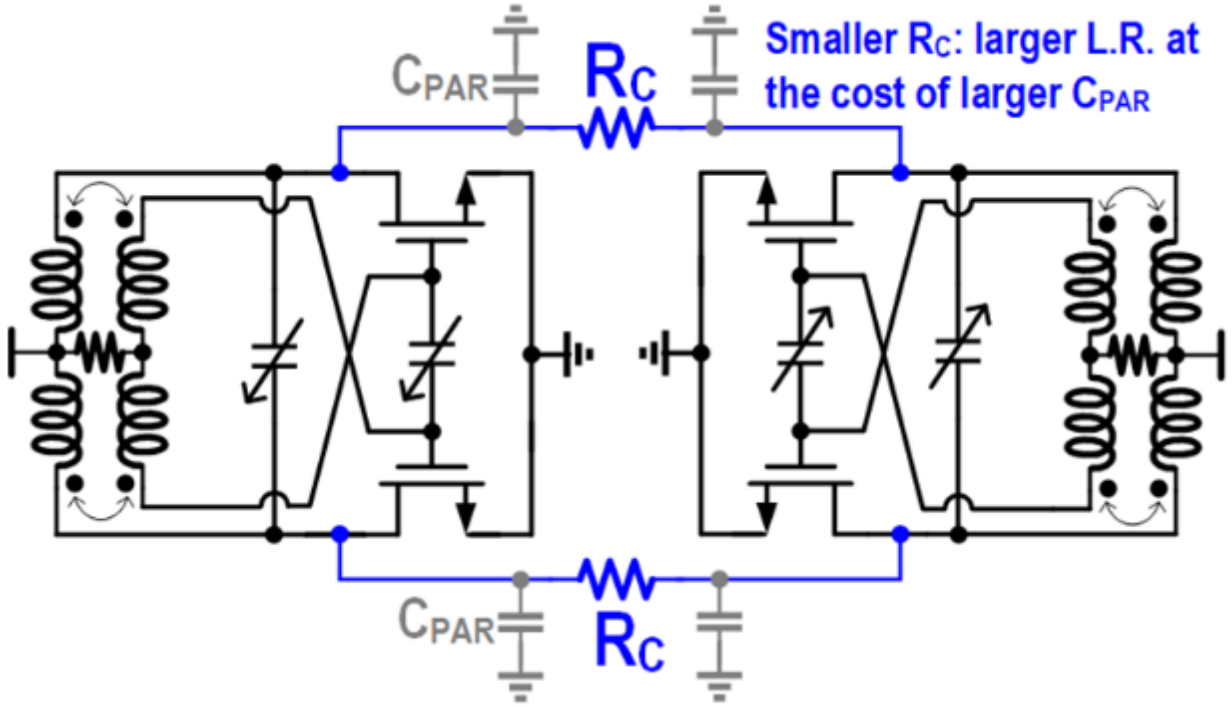
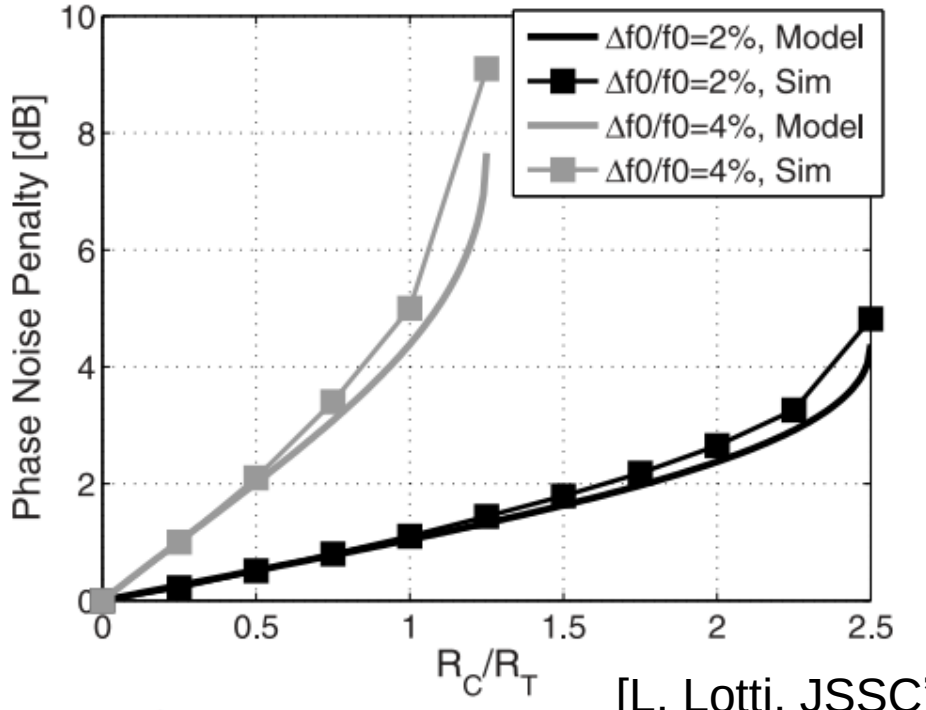
Resistance-Coupled Multi-Core Sync

- ☺ Simple direct connection forces VCO cores to be in-phase
- ☹ One-turn inductor limits the operation frequency
- ☹ Trade-off between mismatch induced PN penalty and C_{PAR}

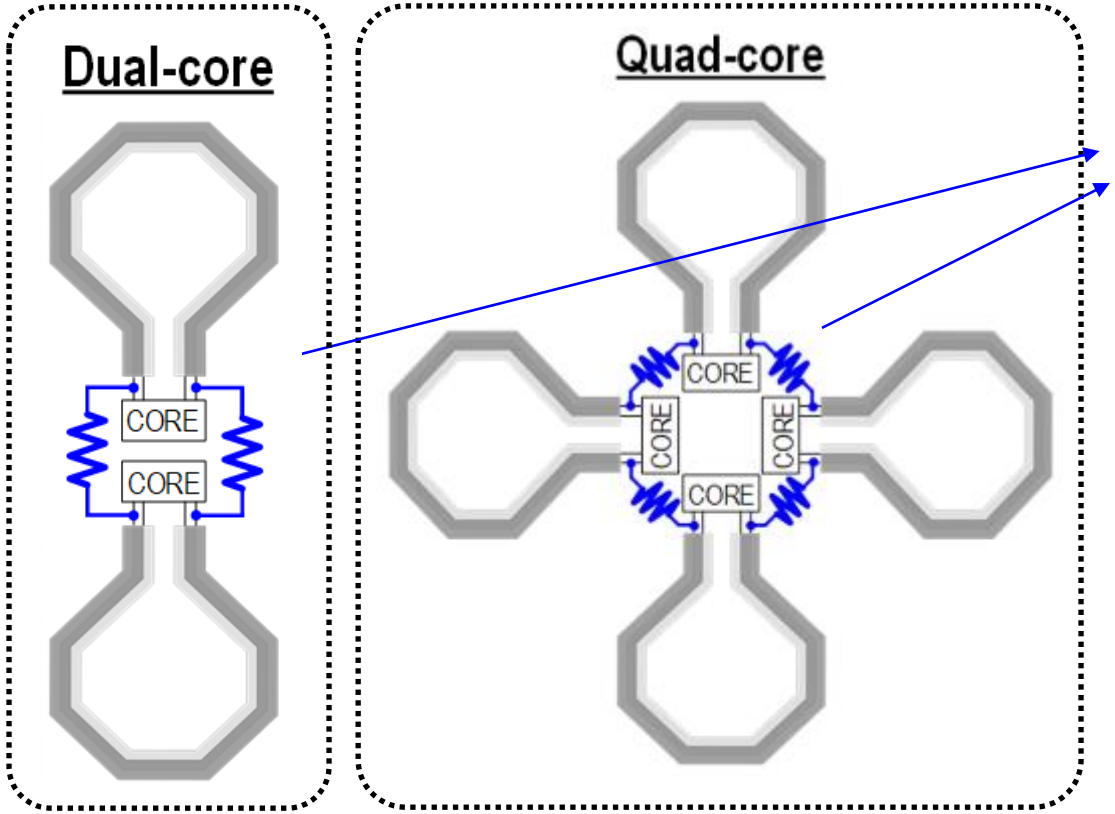




[L. Lotti, JSSC'17]

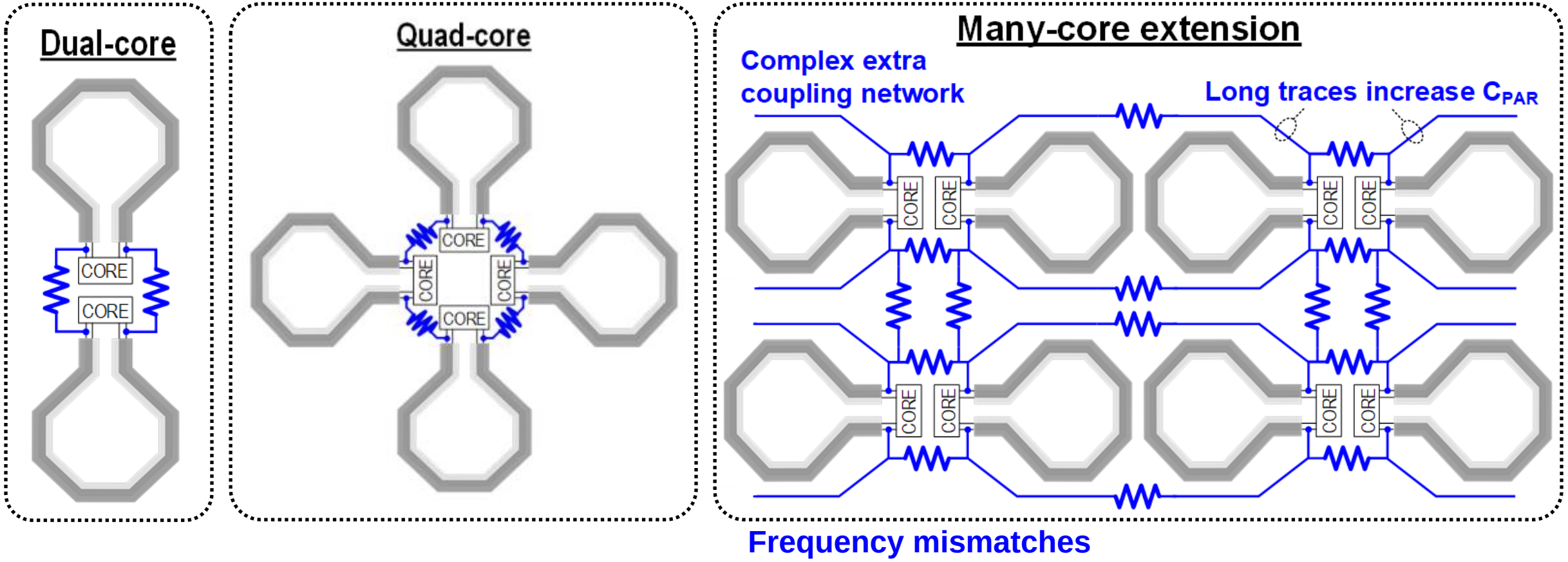
Resistance-Coupled Multi-Core Sync

- **Resistance-Coupled Multi-Core Sync**
  - ☺ **Optimal for RF dual-core or quad-core oscillators**



Resistance-Coupled Multi-Core Sync

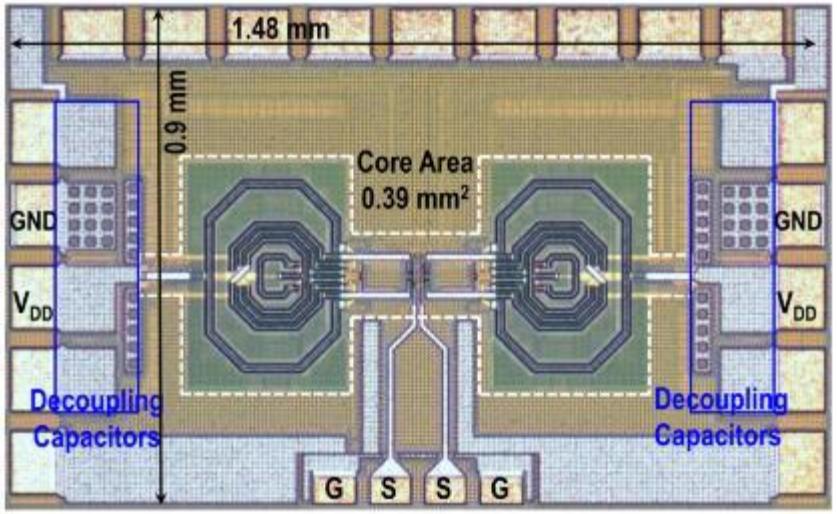
- ☺ Optimal for RF dual-core or quad-core oscillators
- ☹ NOT suitable for many-core due to long coupling traces



Resistance-Coupled Multi-Core Sync

- **Resistance-Coupled Multi-Core Sync**

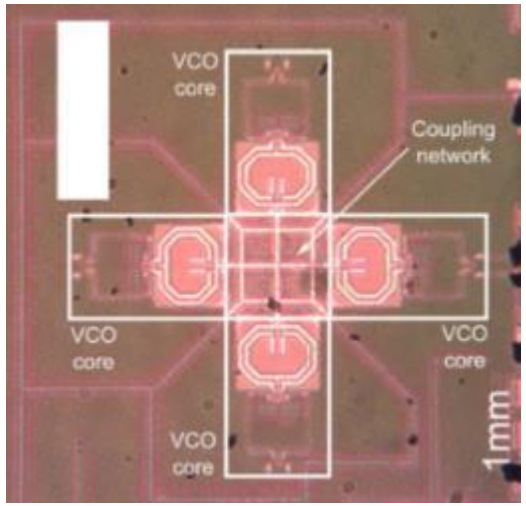
dual-core



22nm FDSOI, **15.1GHz**
-112dBc/Hz PN@1MHz
188dBc/Hz FoM@1MHz

[O. Aassar, JSSC'21]

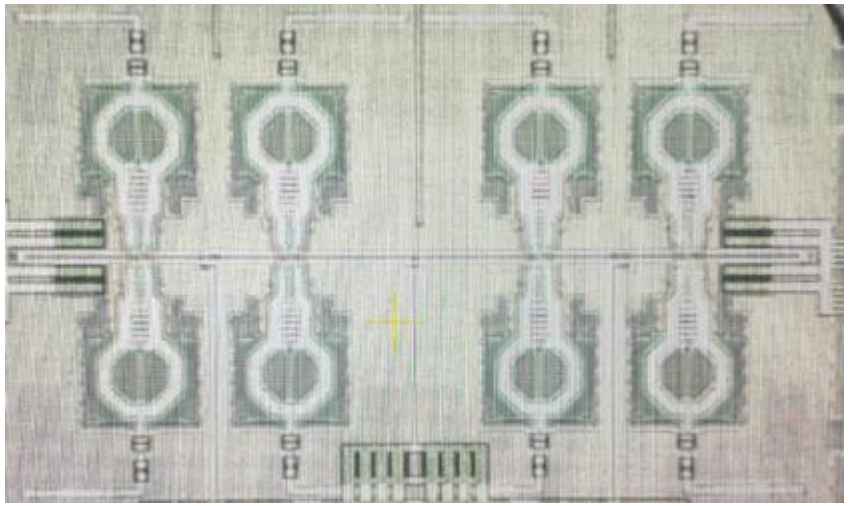
quad-core



130nm BiCMOS, **15.0GHz**
-124dBc/Hz PN@1MHz
189dBc/Hz FoM@1MHz

[F. Padovan, ISSCC'18]

octa-core



28nm CMOS, **10.7GHz**
-126dBc/Hz PN@1MHz
184dBc/Hz FoM@1MHz

[L. Tomasin, RFIC'21]

Resistance-Coupled Multi-Core Sync

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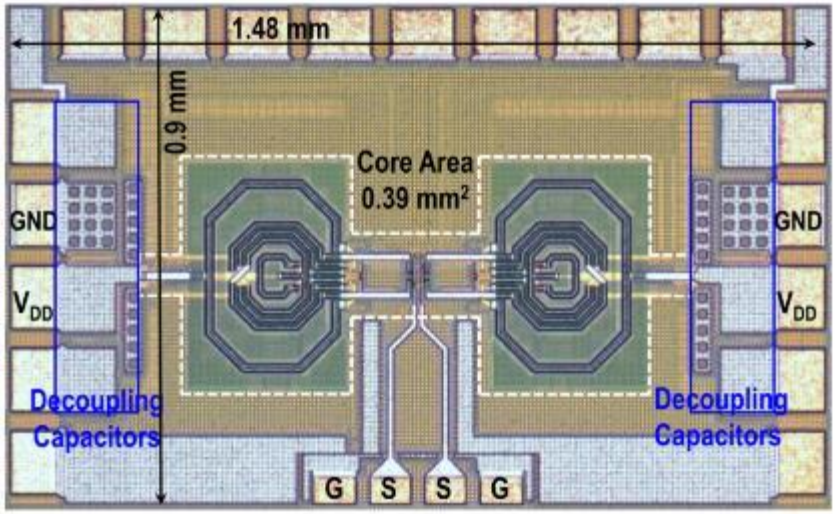
dual-core



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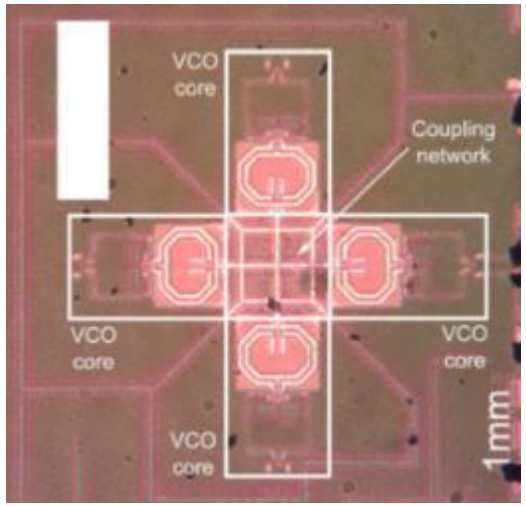

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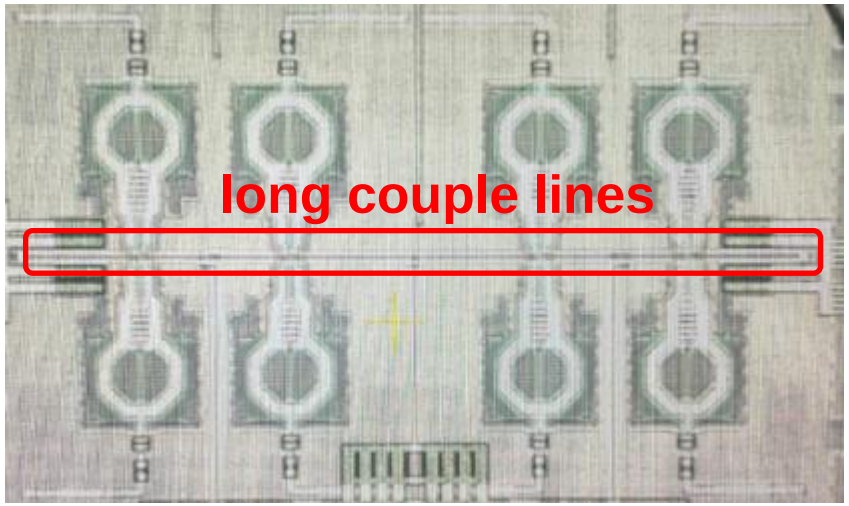
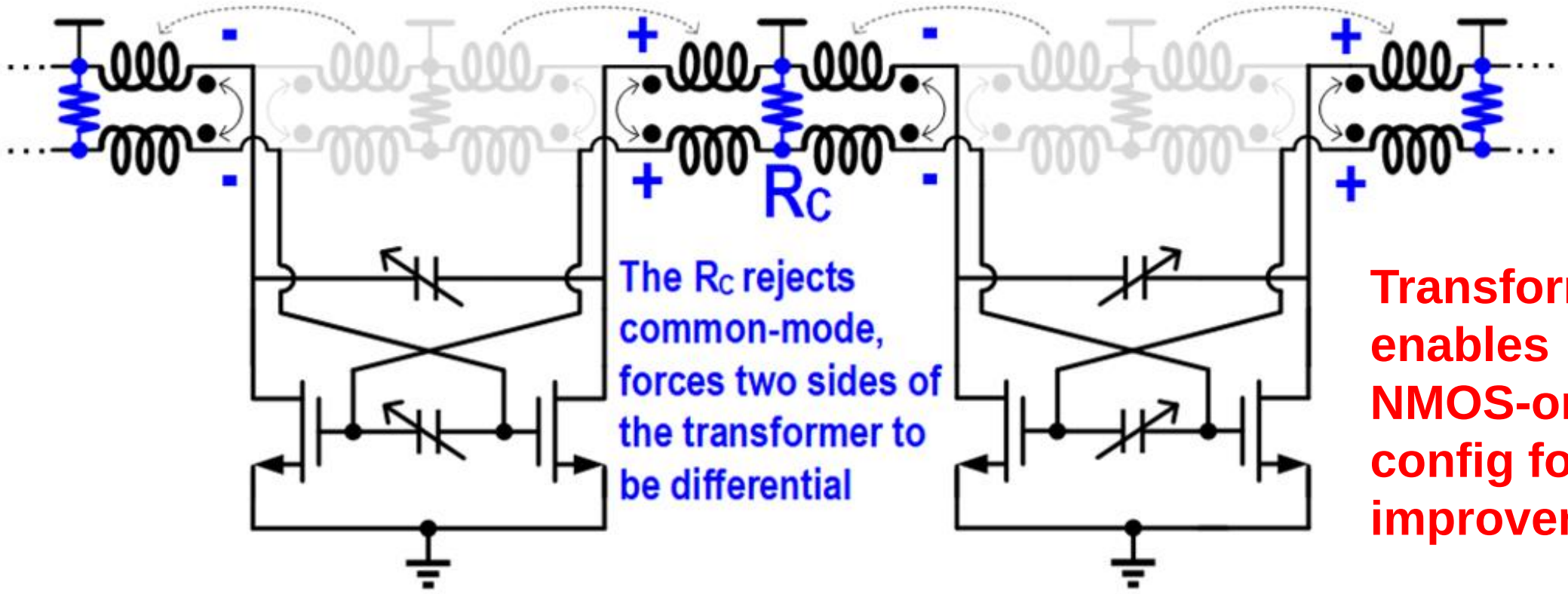


28nm CMOS, **10.7GHz**
-126dBc/Hz PN@1MHz
184dBc/Hz FoM@1MHz

[L. Tomasin, RFIC'21]

Mode-Rejection-Coupled Multi-Core Sync

- Each differential pair shares transformer with adjacent ones
- CM current flows through R_C, reducing Q_{CM}, forcing differential

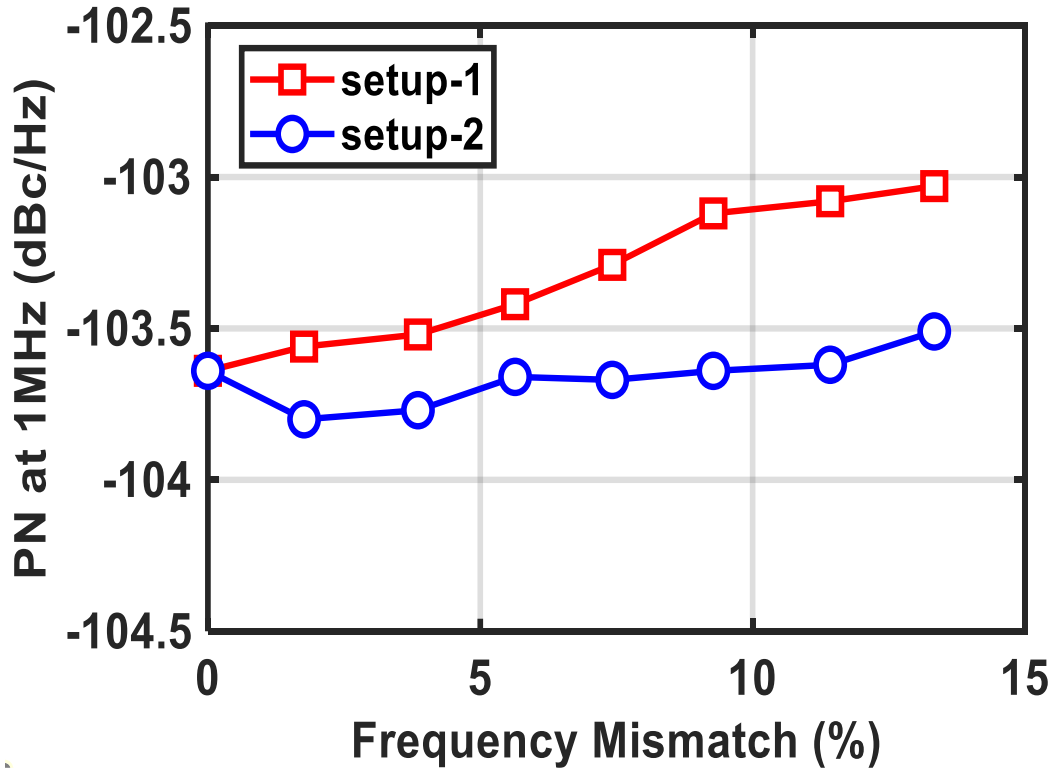


Transformer enables NMOS-only config for PN improvement

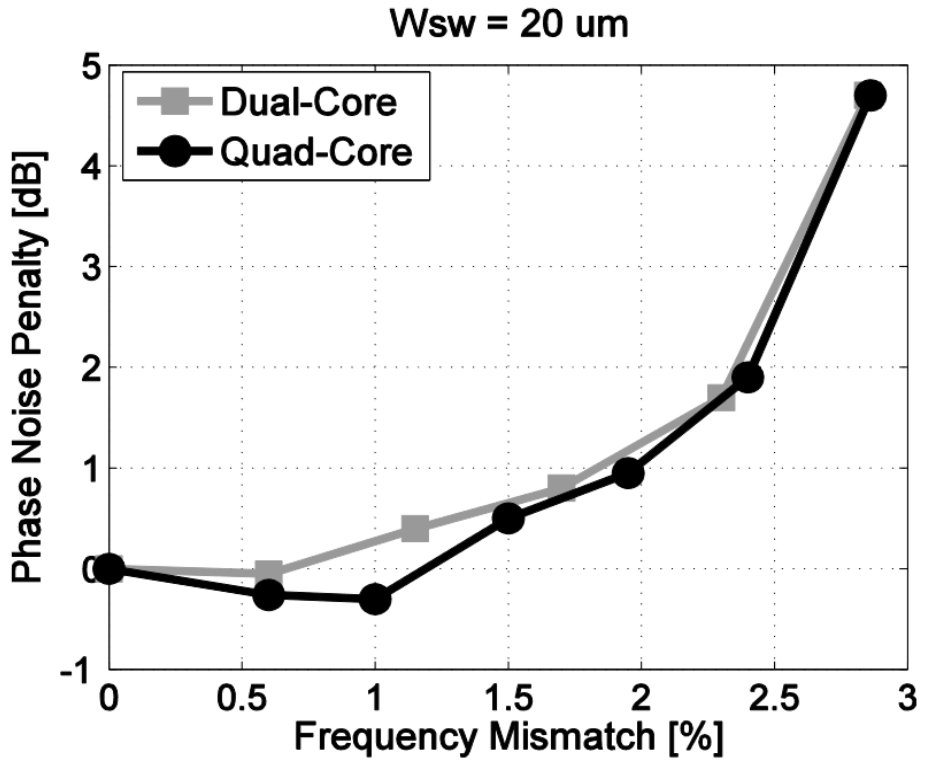
Mode-Rejection-Coupled Multi-Core Sync

- **Better performance against frequency mismatches**

Mode-Rejection-Coupled



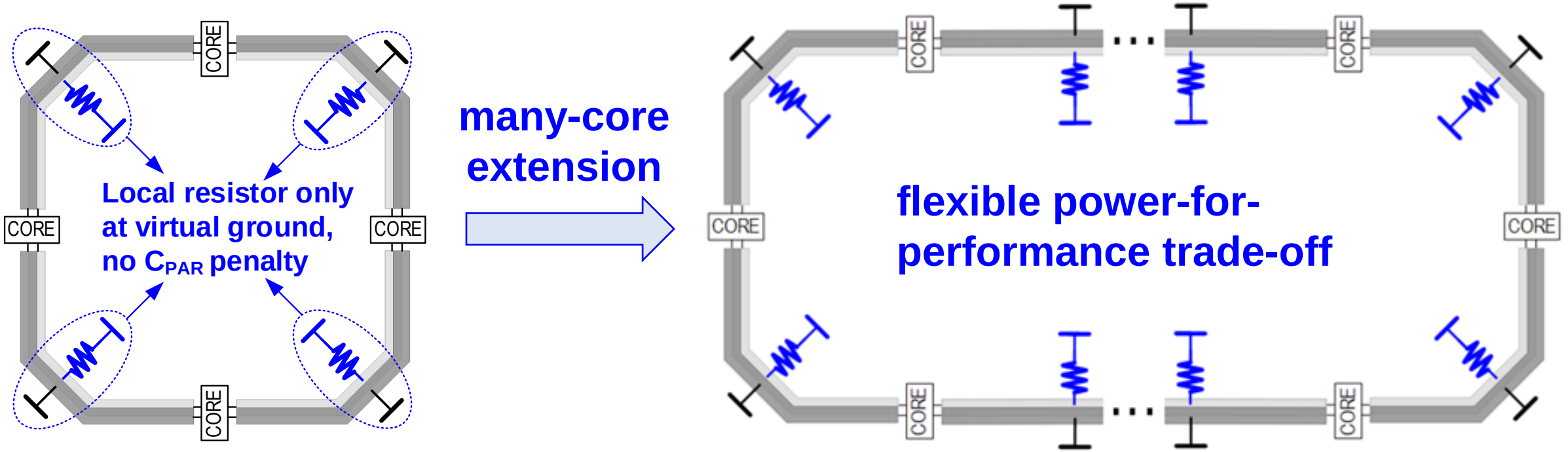
Resistance-Coupled



[L. Lotti, JSSC'17]

A Better Choice for Many-Core Oscillator

- **Mode-Rejection-Coupled Multi-Core Sync**
  - ☺ **Only local resistors at virtual ground, no C_{PAR} penalty**
  - ☺ **Easy extend to many-core oscillators**



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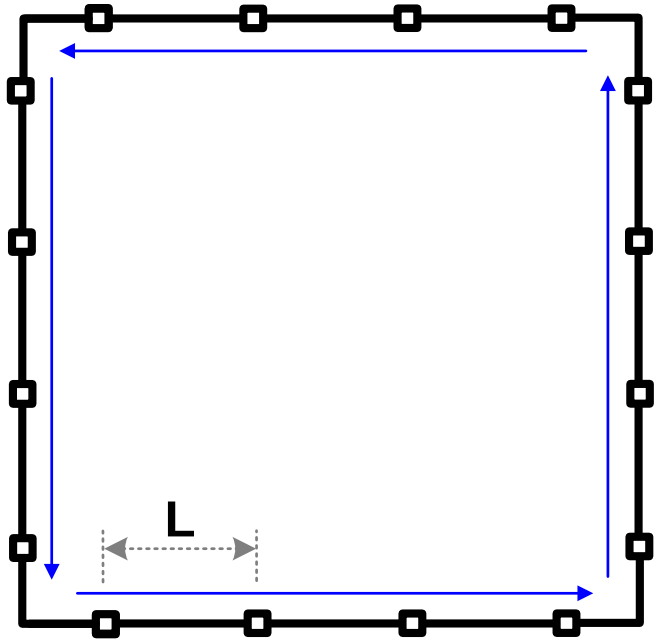
Many-Core Oscillator Floorplan

- Series topology many-core floorplan
- Large chip area and long power deliver distance from outside

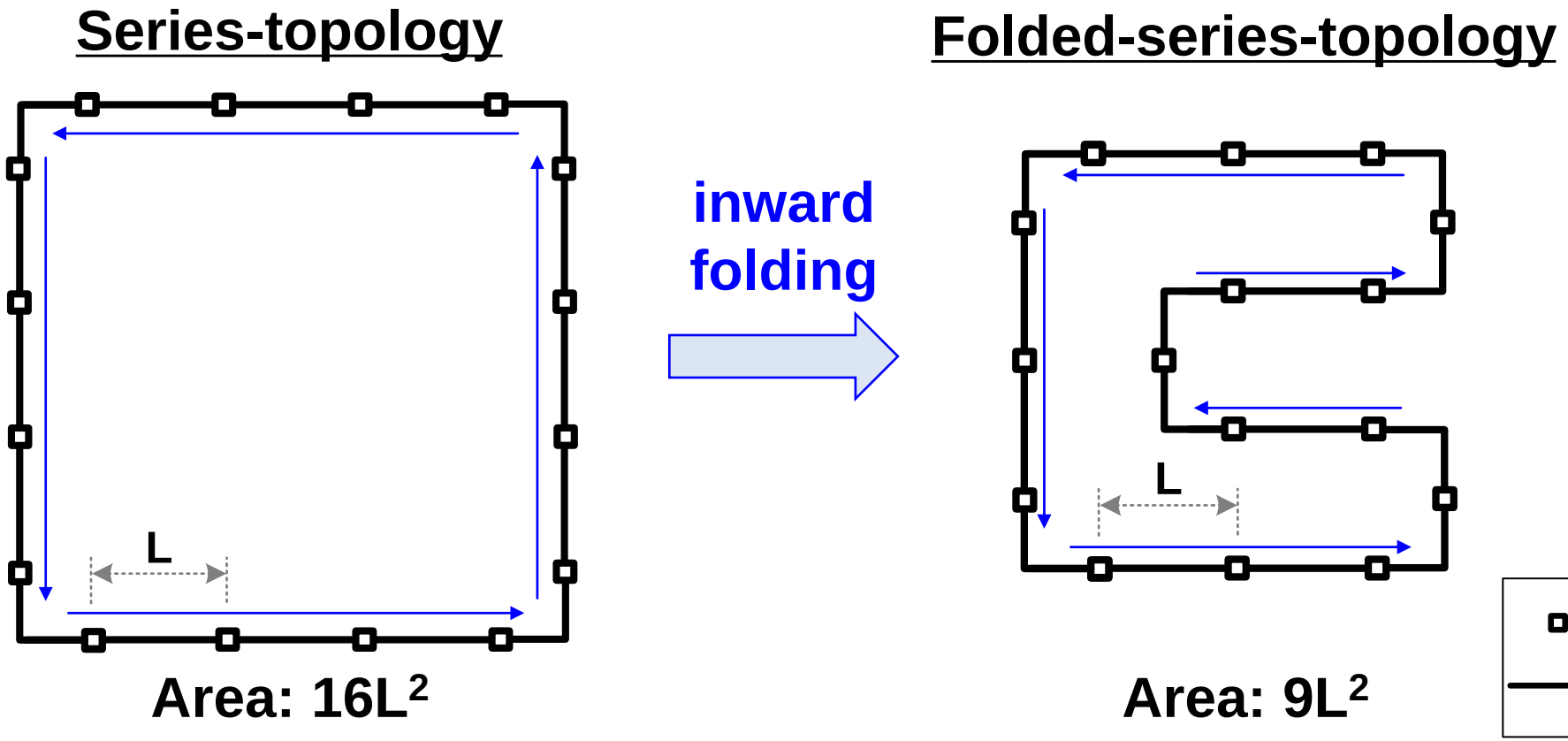
Series-topology



Area: $16L^2$

Many-Core Oscillator Floorplan

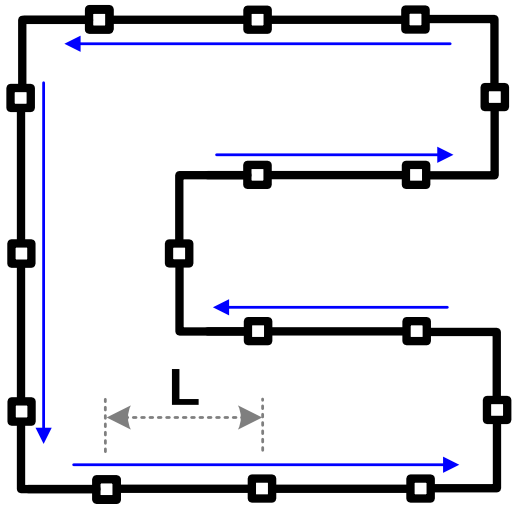
- Folded-series topology many-core floorplan
- Inward folding to make use of inner empty spaces



Proposed Mesh-Topology Floorplan

- Make fully use of inner grid edges to route transformers
- Corner space available for DECAP or other circuity

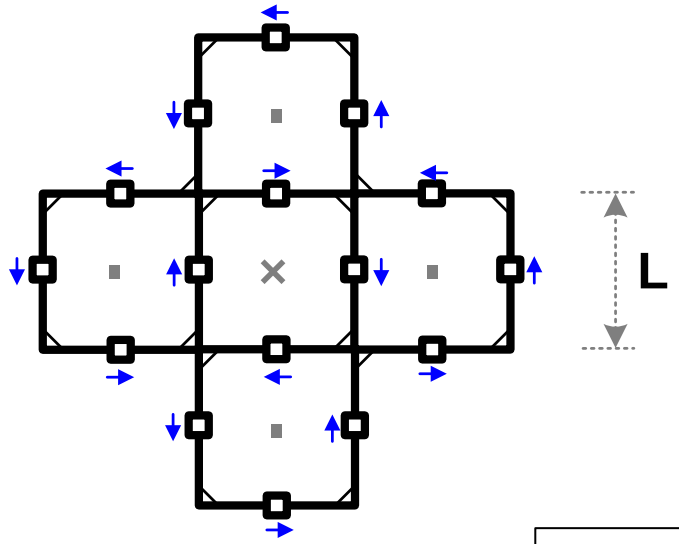
Folded-series-topology



Area: $9L^2$

further improvement

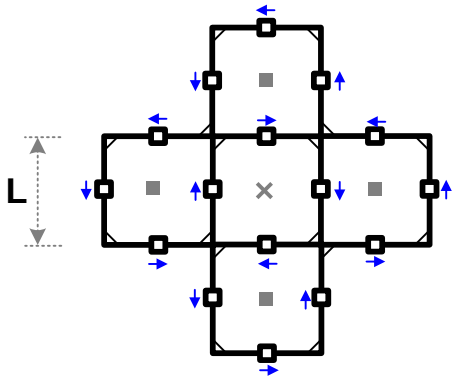
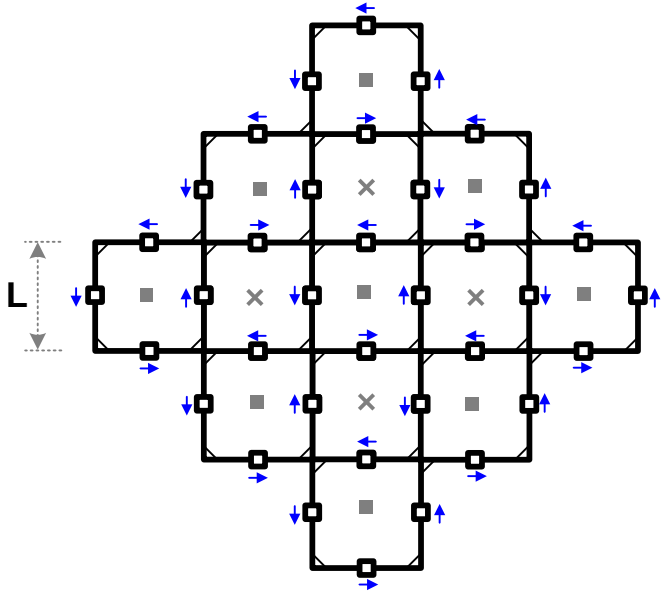
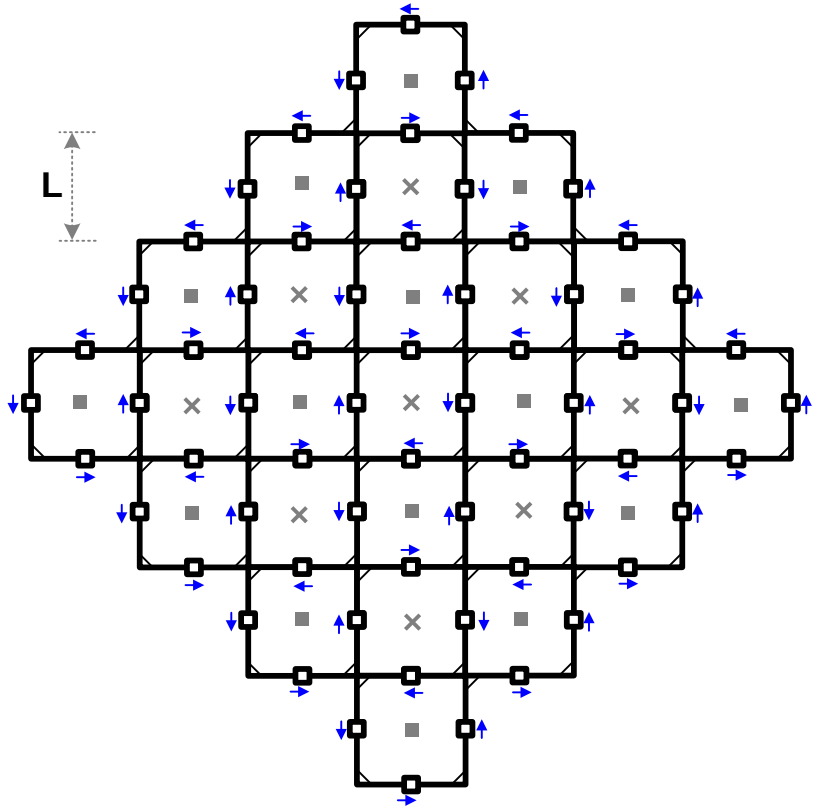
Mesh-topology



Area: $5L^2$

Proposed Mesh-Topology Floorplan

- **Scalable for flexible power-for-performance trade-off**

16-core	36-core	64-core
VCO core Transformer 	core area=$\frac{\left(\sqrt{N}-1\right)^2+1}{2}$ 	
core area: $5L^2$	core area: $13L^2$	core area: $25L^2$

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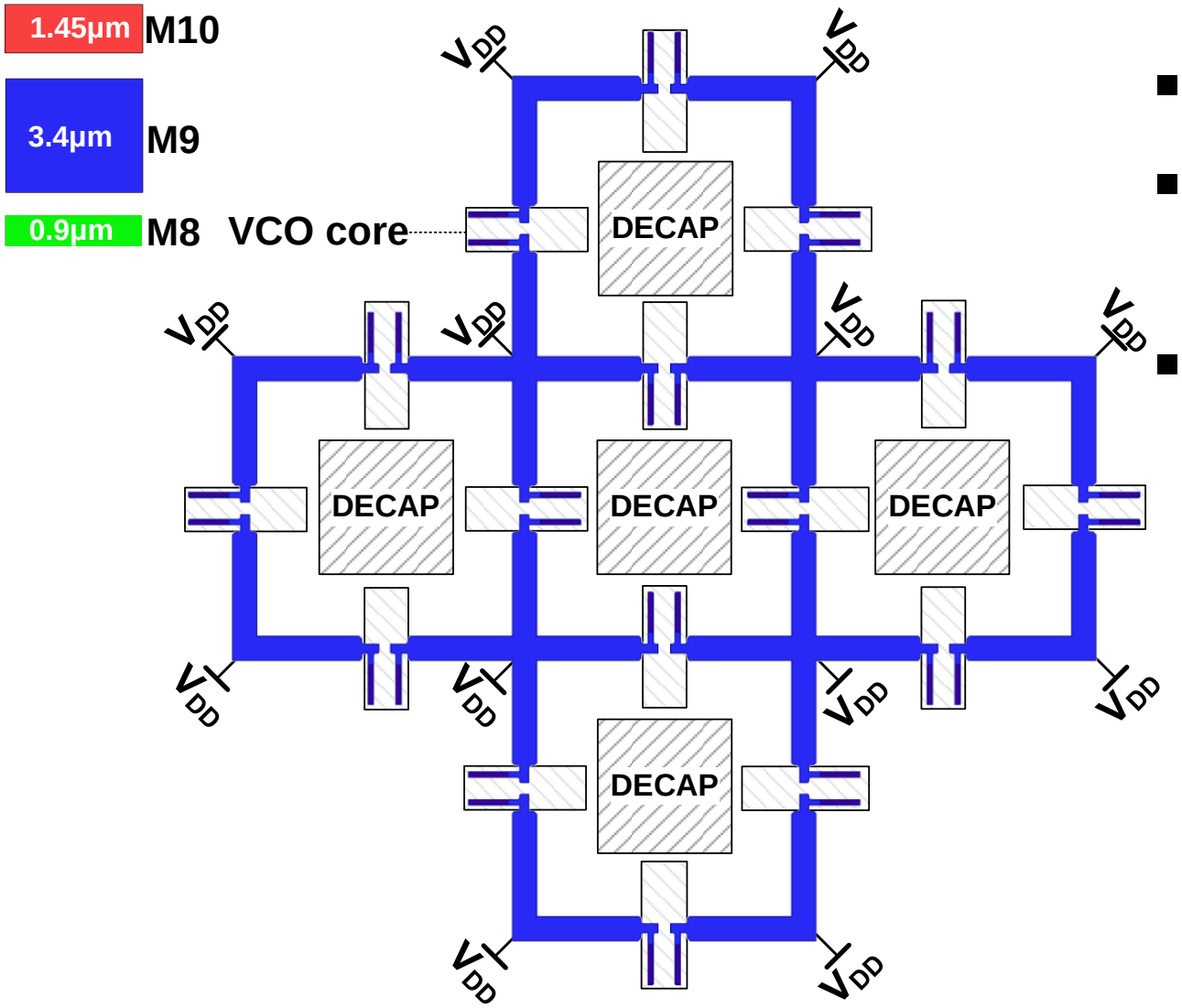
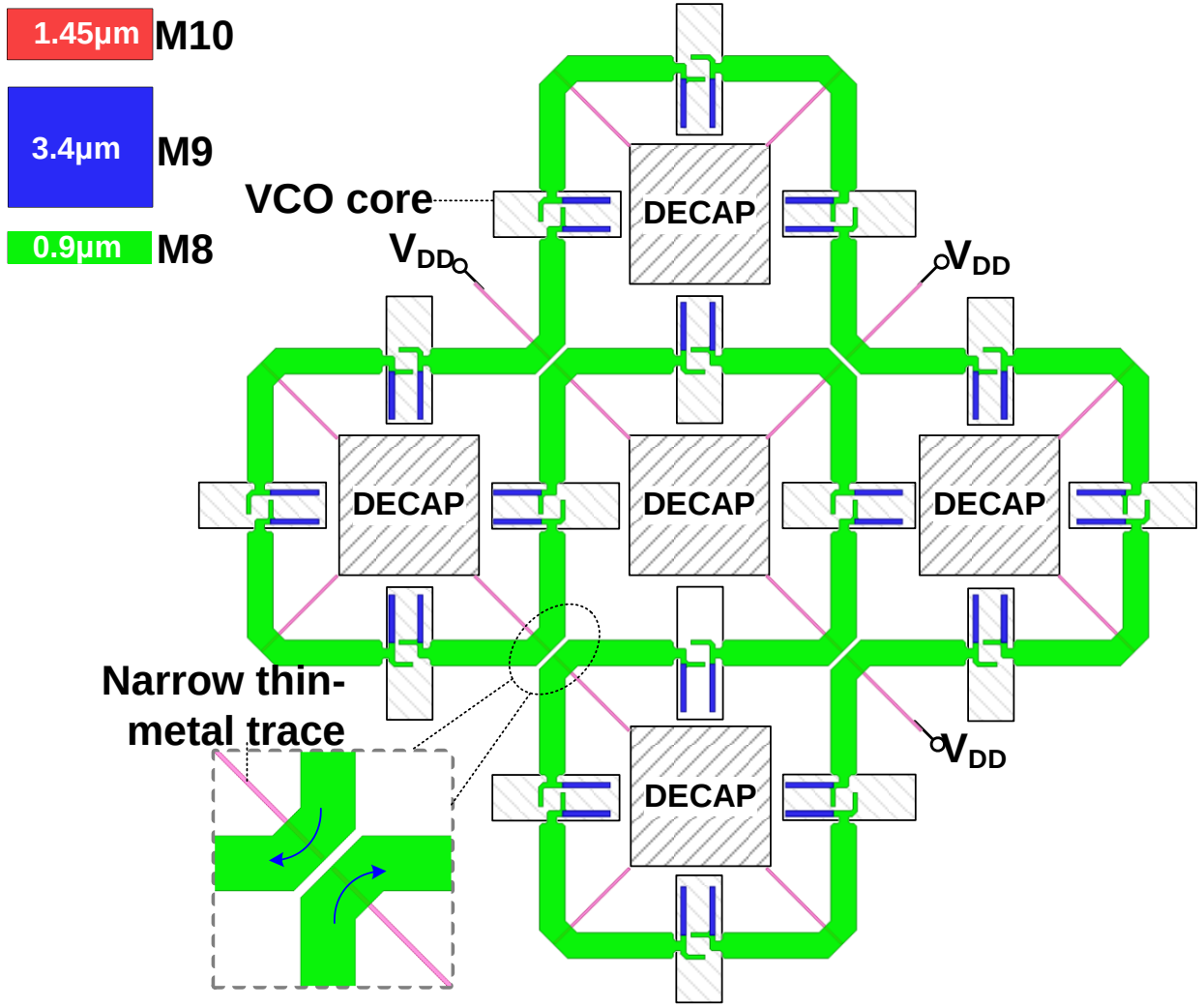
The Mesh-Topology Transformers



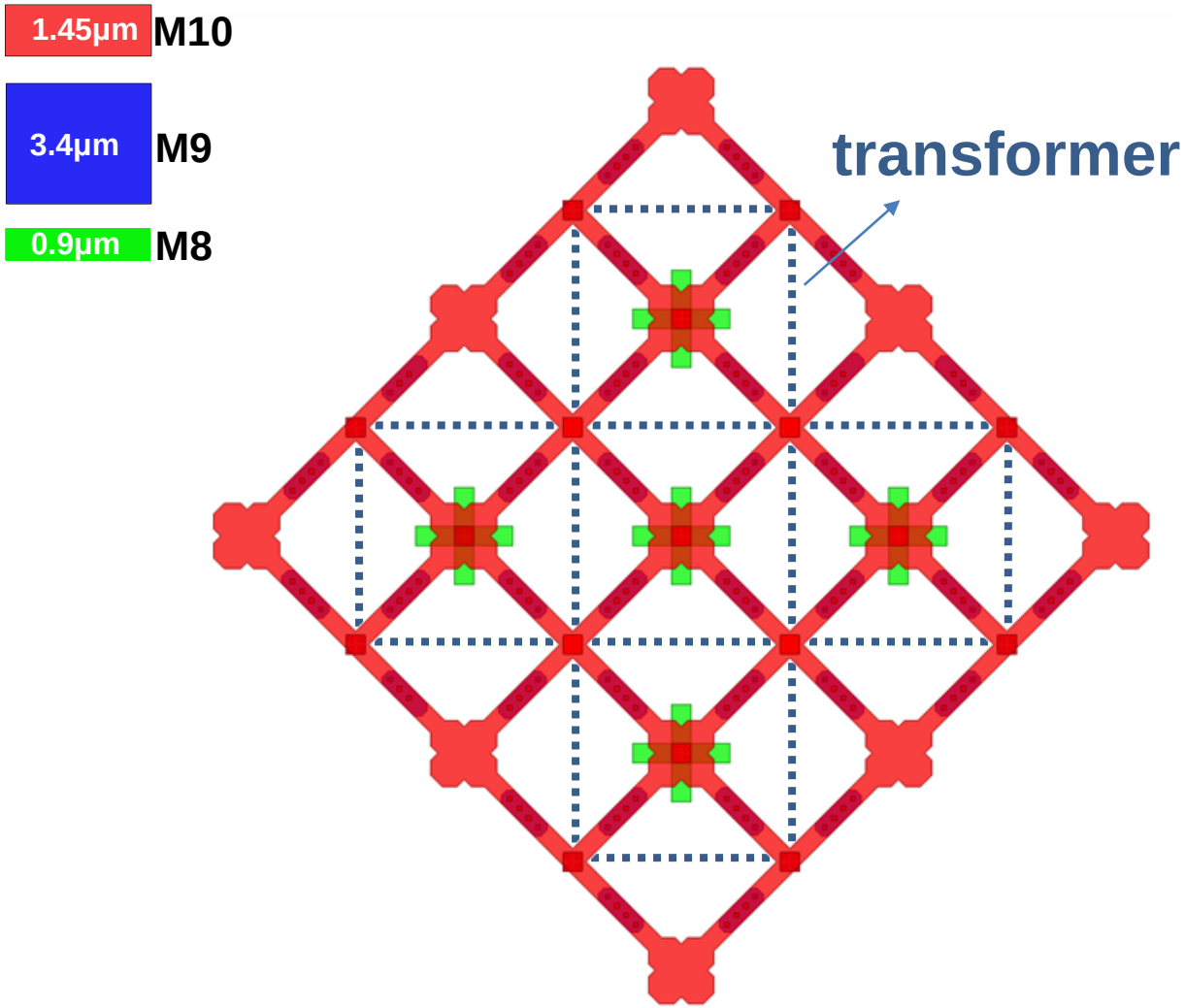
- Transformer coil at drains
- The thick most 3.4μm M9 chosen for IR drop consideration
- Supply power at all central taps

The Mesh-Topology Transformers



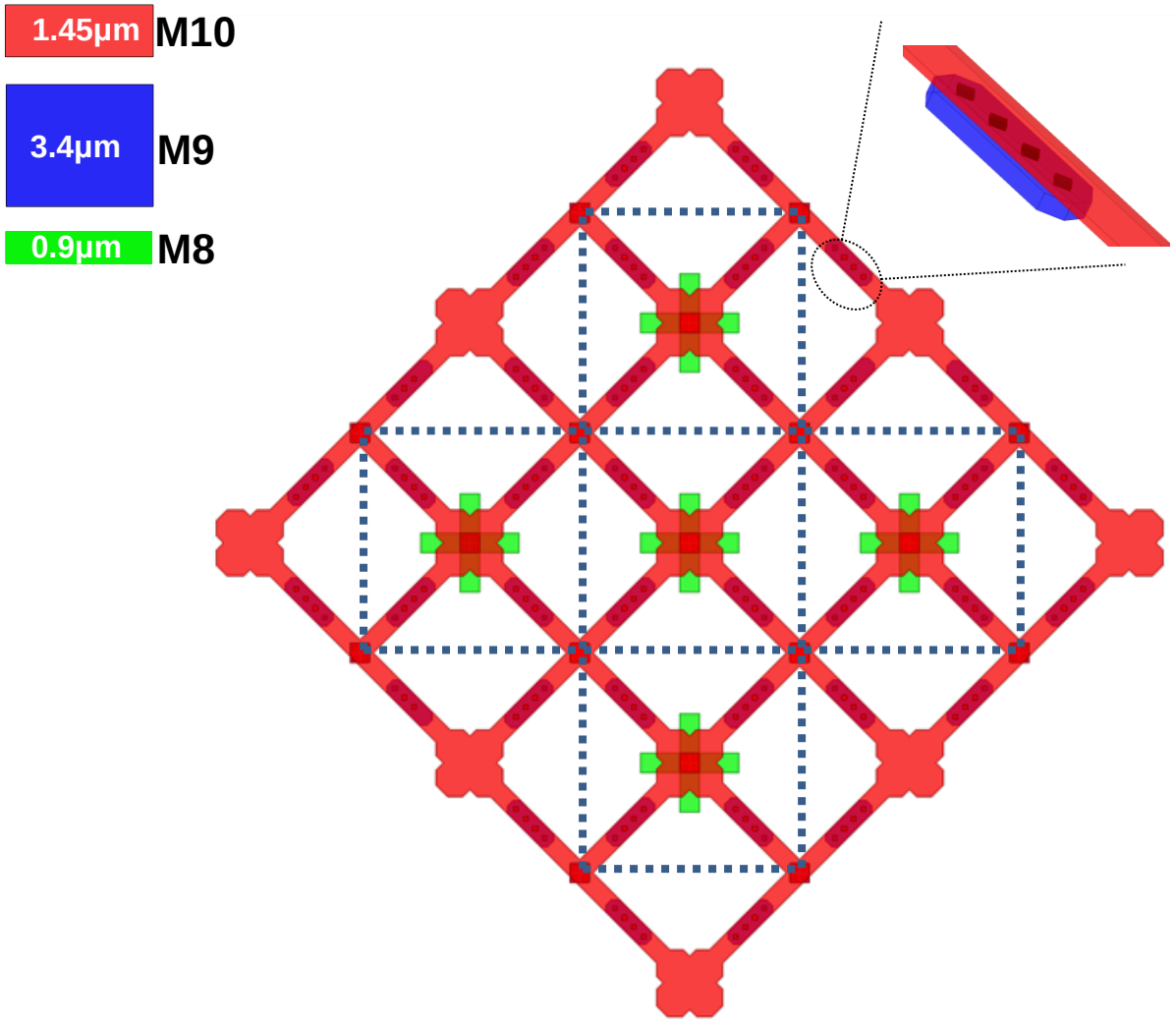
- Transformer coil at gates
- The 0.9μm M8 layer is chosen
- Split at the mesh cross points
- Common-mode rejection and gate dc bias realized by narrow thin-metal trace resistance

Power Delivery Network (V_{DD})



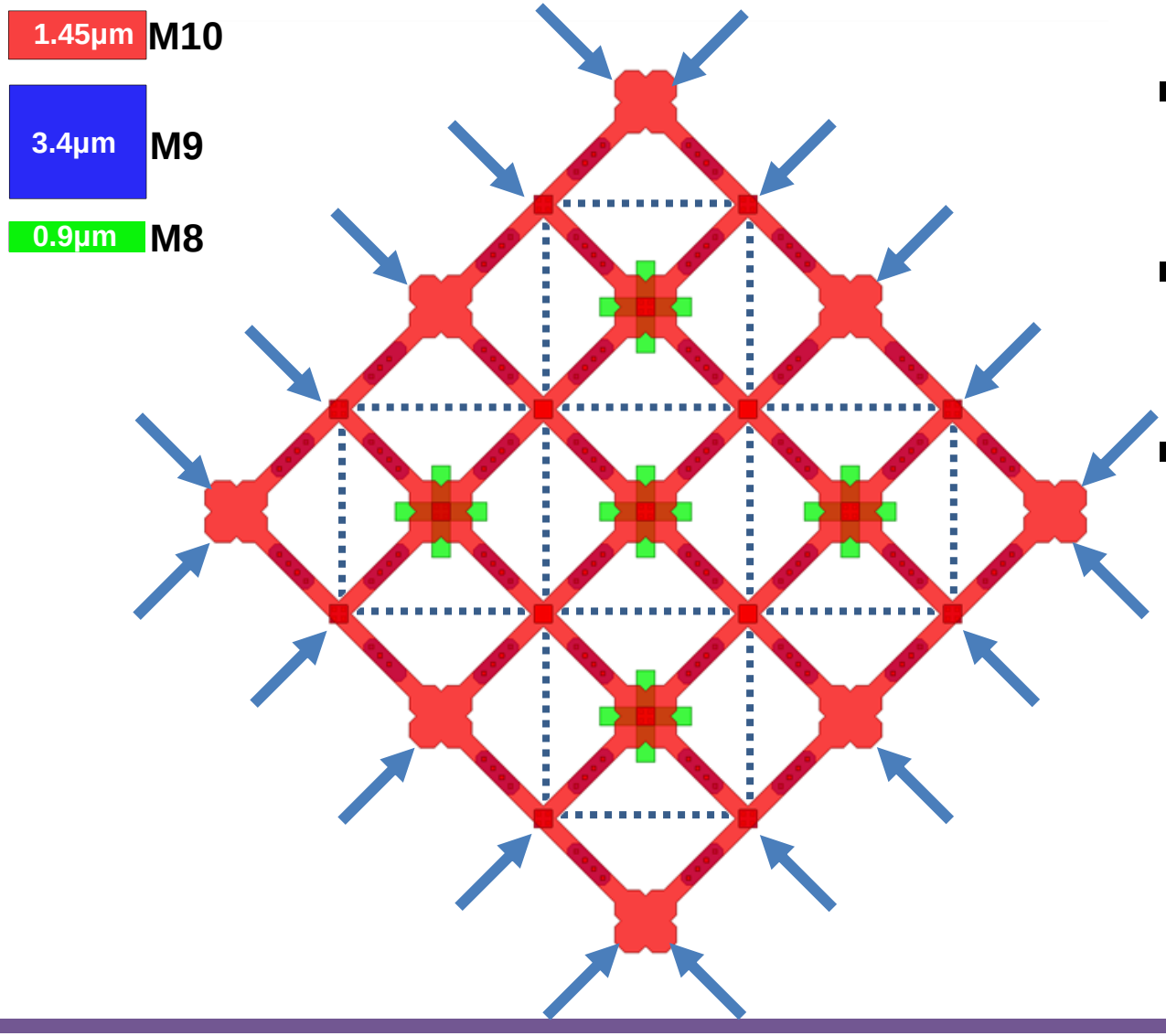
- Diamond-shape V_{DD} network to avoid overlap with transformers

Power Delivery Network (V_{DD})



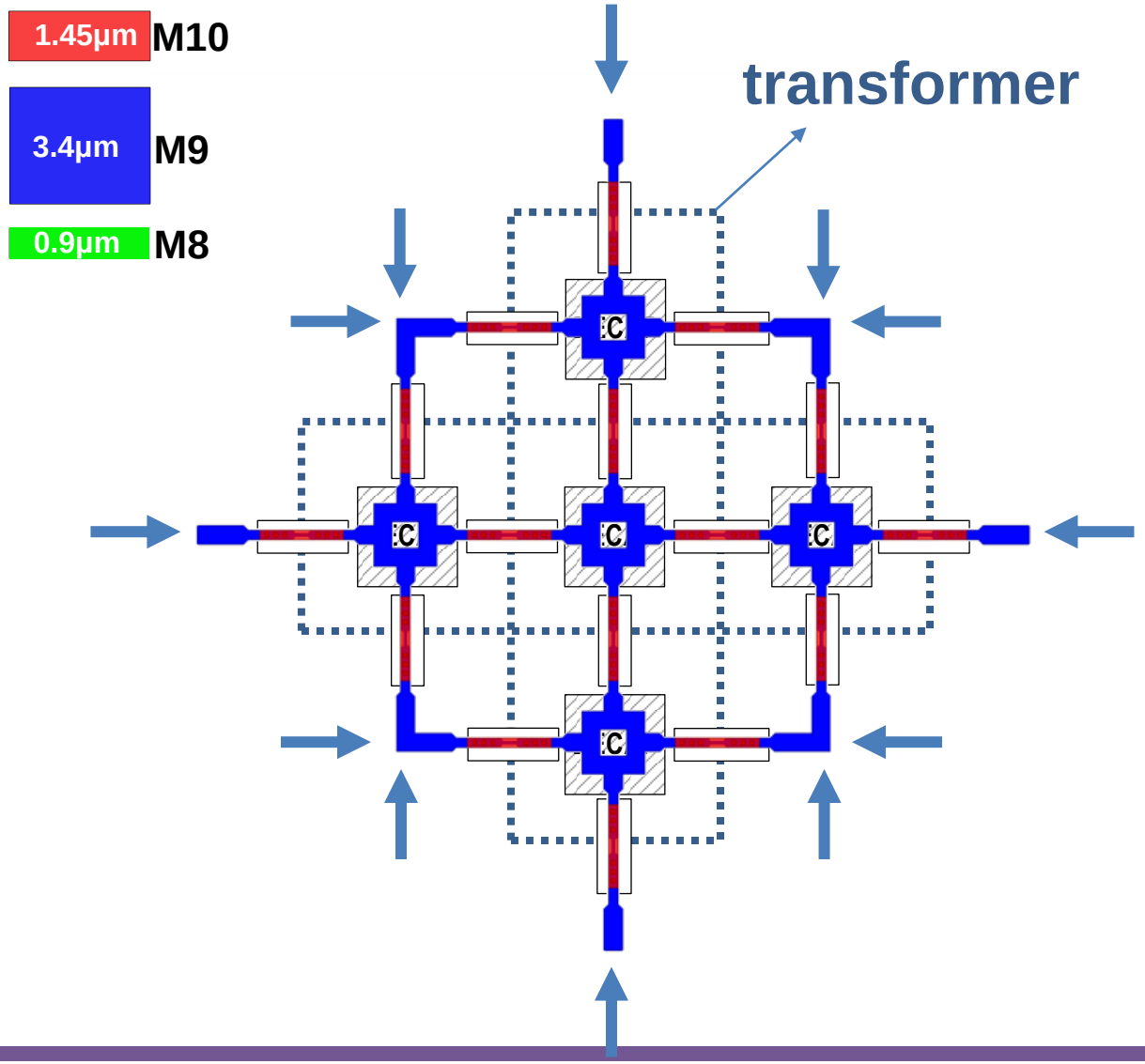
- Diamond-shape V_{DD} network to avoid overlap with transformers
- Mainly use 1.45µm M10, stacking 3.4µm M9 when possible

Power Delivery Network (V_{DD})



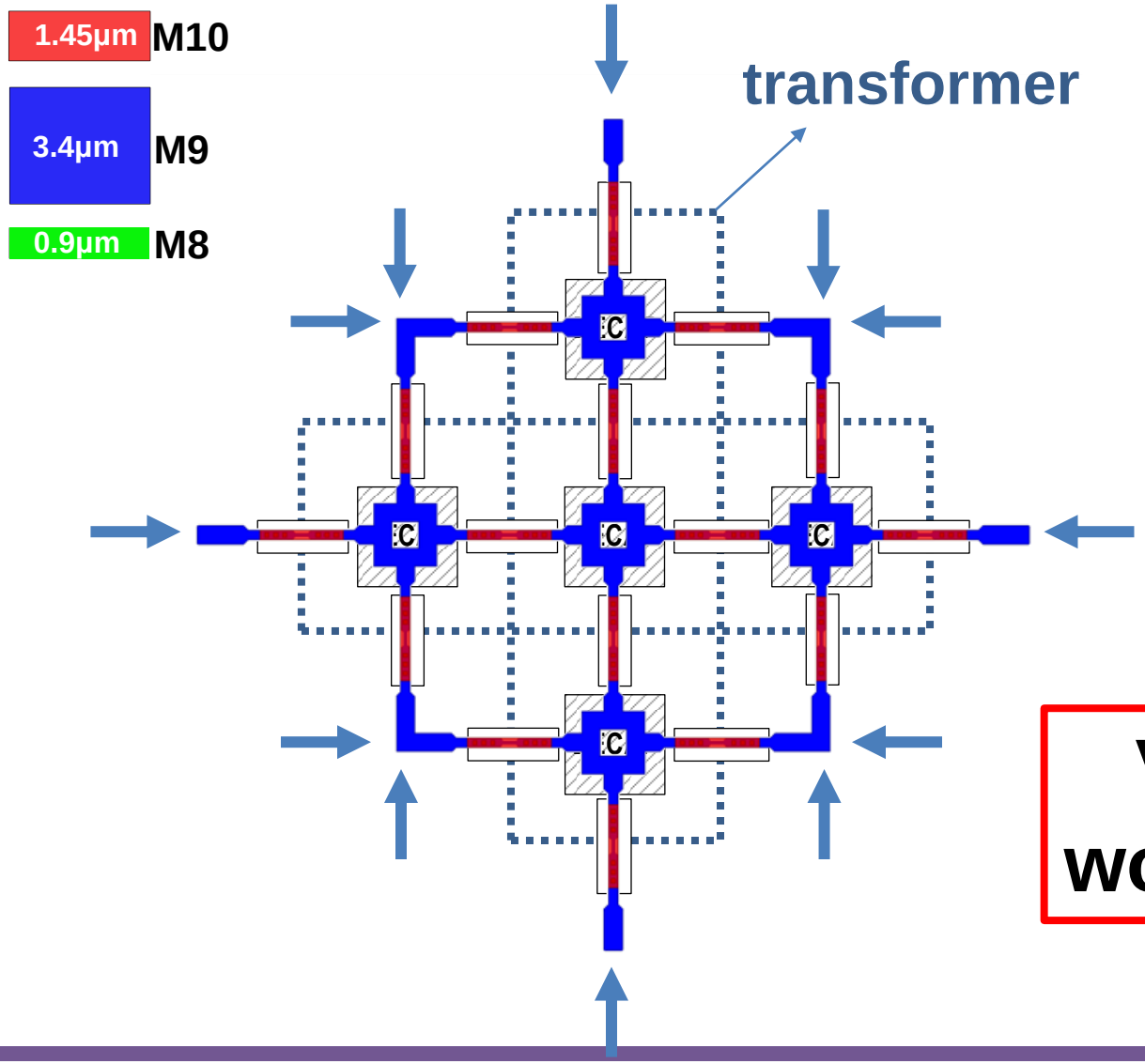
- Diamond-shape V_{DD} network to avoid overlap with transformers
- Mainly use 1.45μm M10, stacking 3.4μm M9 when possible
- Distributed outsider access point to reduce IR drop

Power Delivery Network (V_{SS})



- V_{SS} network perpendicular to transformers
- Mainly use 3.4µm M9, stacking 1.45µm M10 when possible
- Distributed outsider access point to reduce IR drop

Power Delivery Network (V_{SS})

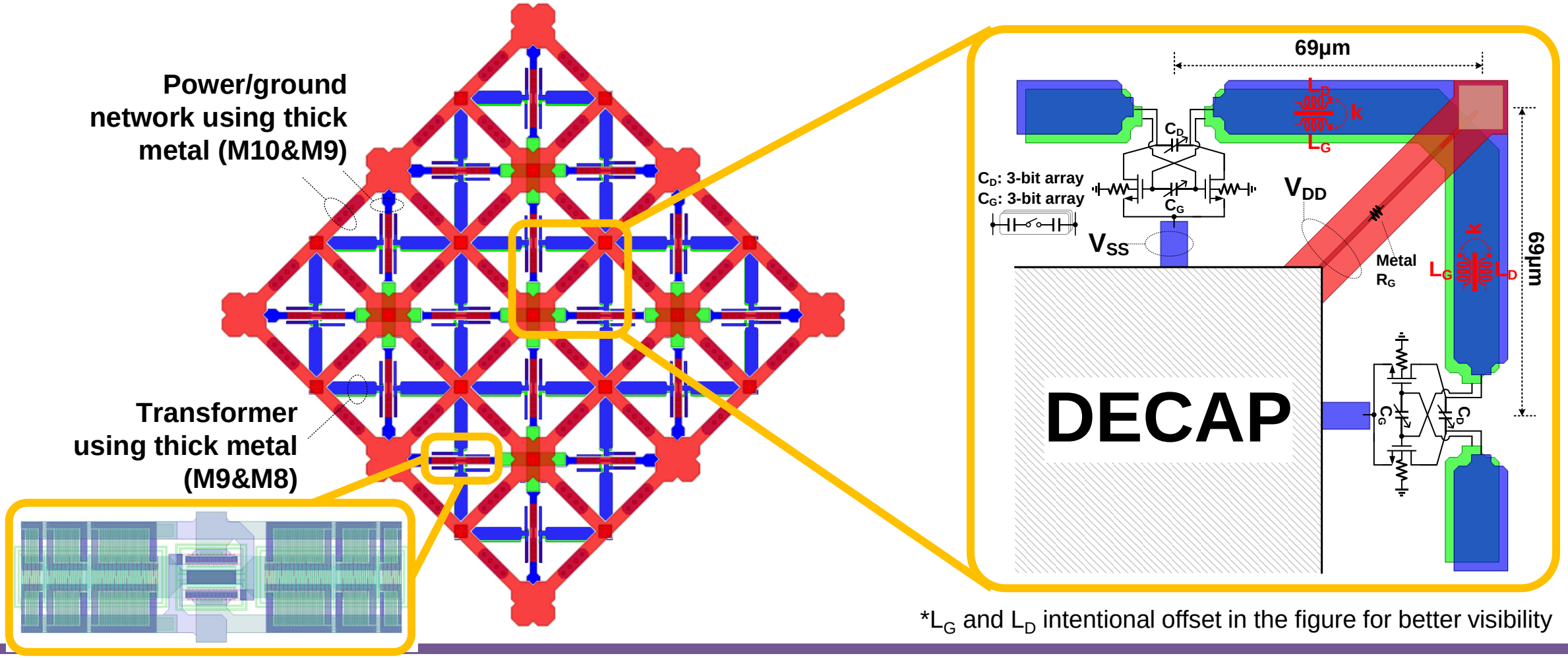


- V_{SS} network perpendicular to transformers
- Mainly use 3.4µm M9, stacking 1.45µm M10 when possible
- Distributed outsider access point to reduce IR drop

V_{DD} and V_{SS} combined 4.2mV worst IR drop in post-simulation

Tile-Based Single Oscillator Core

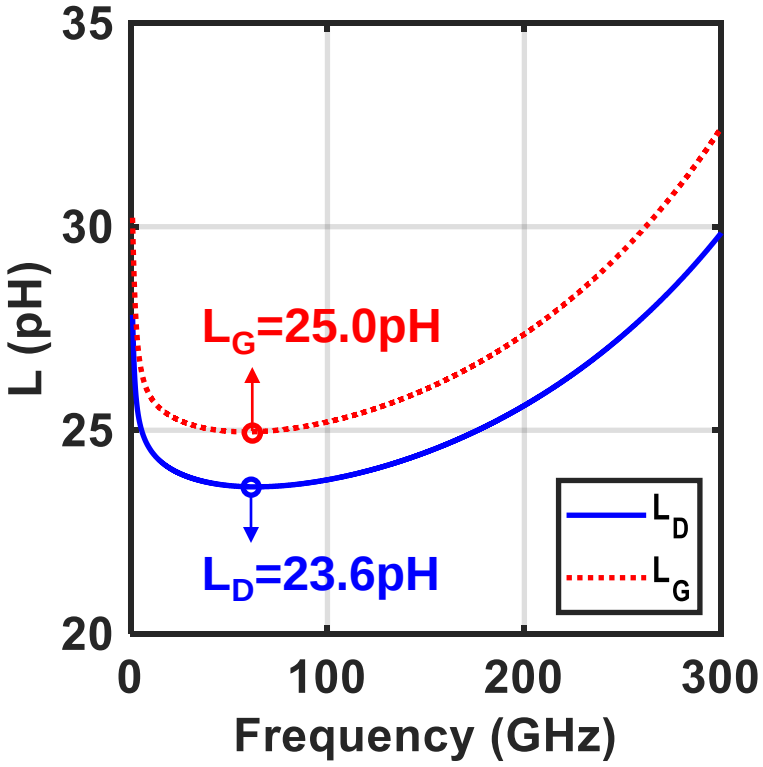
- **Reusable tile-based oscillator core to save layout effort**

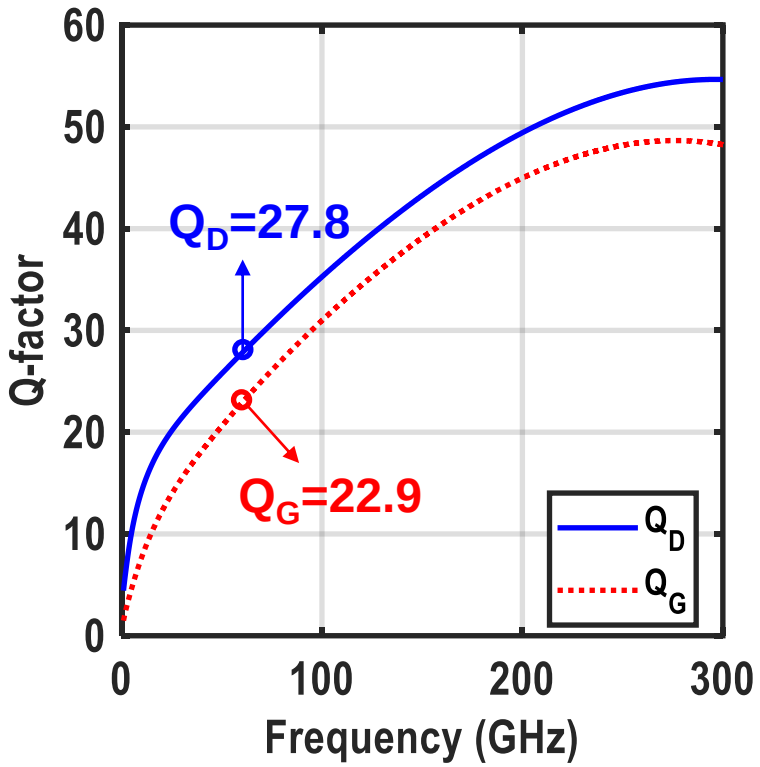


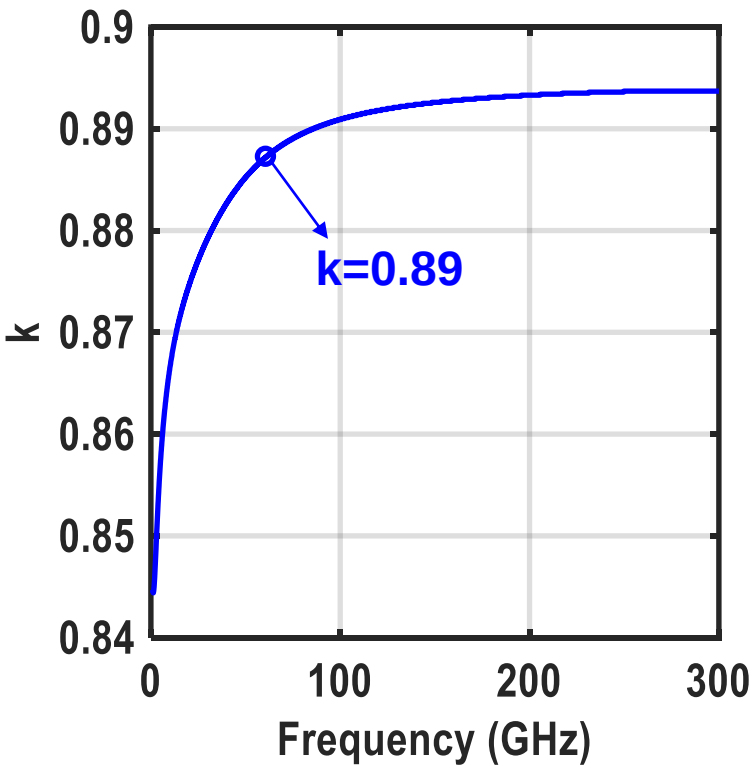
*L_G and L_D intentional offset in the figure for better visibility

Tile Transformer Simulated Results

- Inductance of <25pH and Q of >22 at 60GHz achieved
- L_D and L_G strongly coupled (k=0.89 at 60GHz)



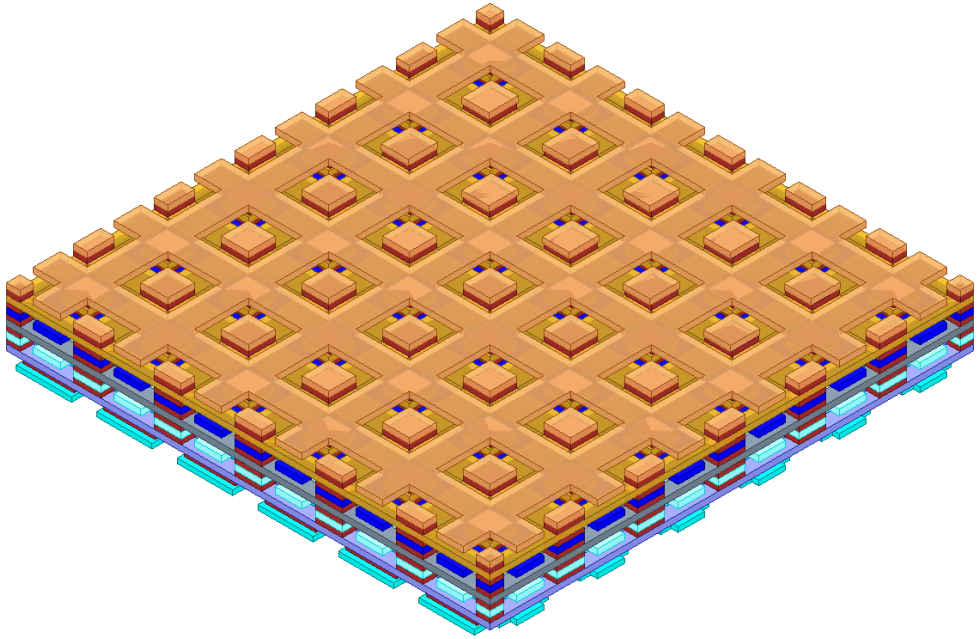


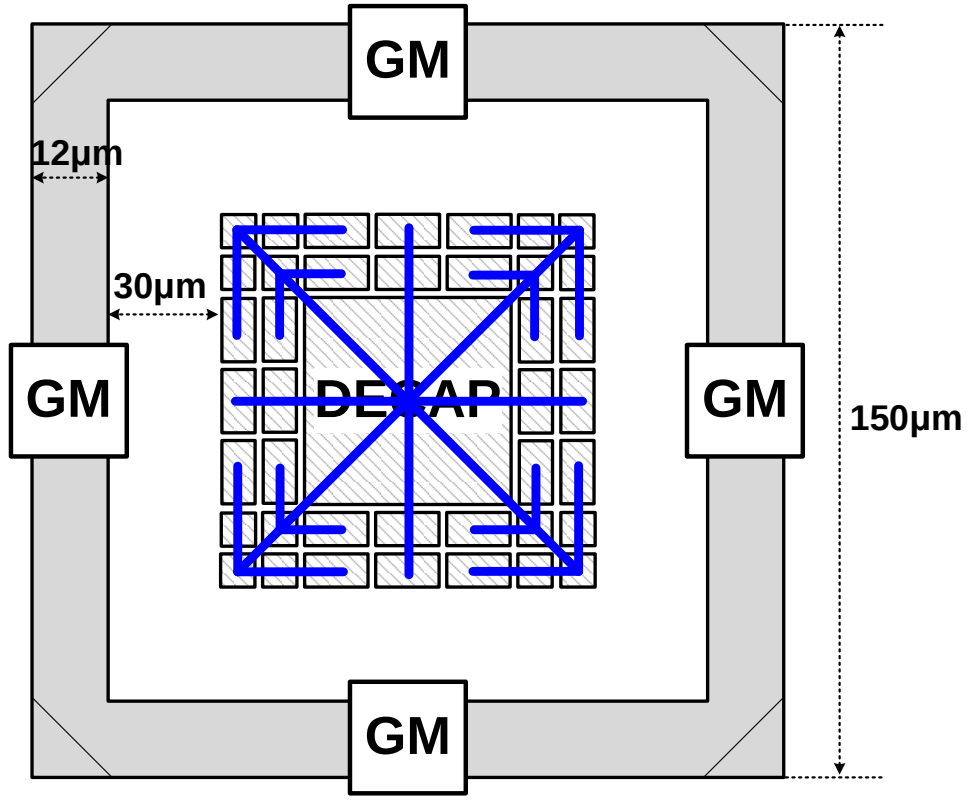


Decoupling Capacitor Implementation

- Combination of high-Q MOM and low-Q MOS capacitor
- Partially pattern ground shield style not to degrade tank's Q

8.5pF total
6.9pF MOS
1.6pF MOM
~2.0fF/μm²

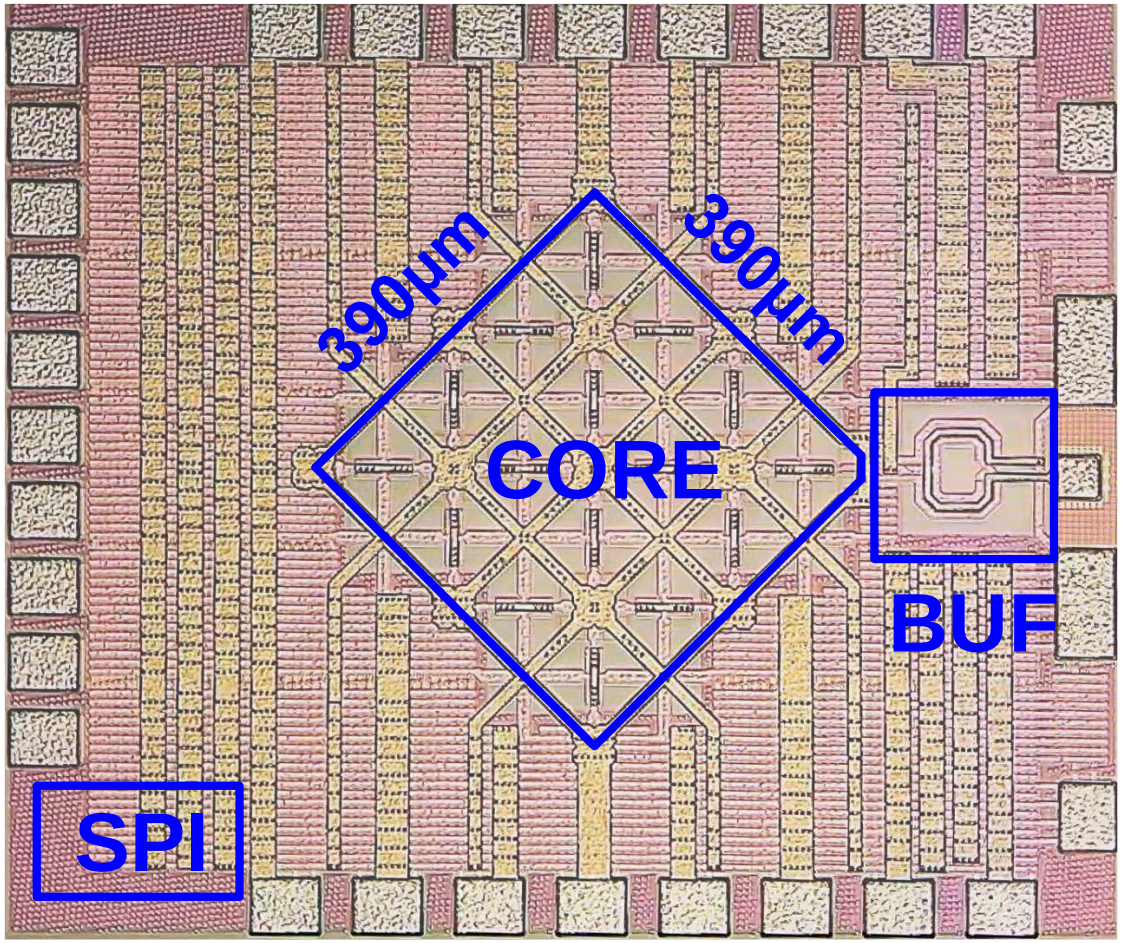




Outline

- Introduction
- Challenges for mm-Wave High-Quality VCOs
- From Multi-Core to Many-Core
  - Synchronization Methods
  - Core Floorplan
- **Mesh-Topology 16-Core Oscillator Prototype**
  - Implementation Details
  - **Measured Results**
- Conclusions

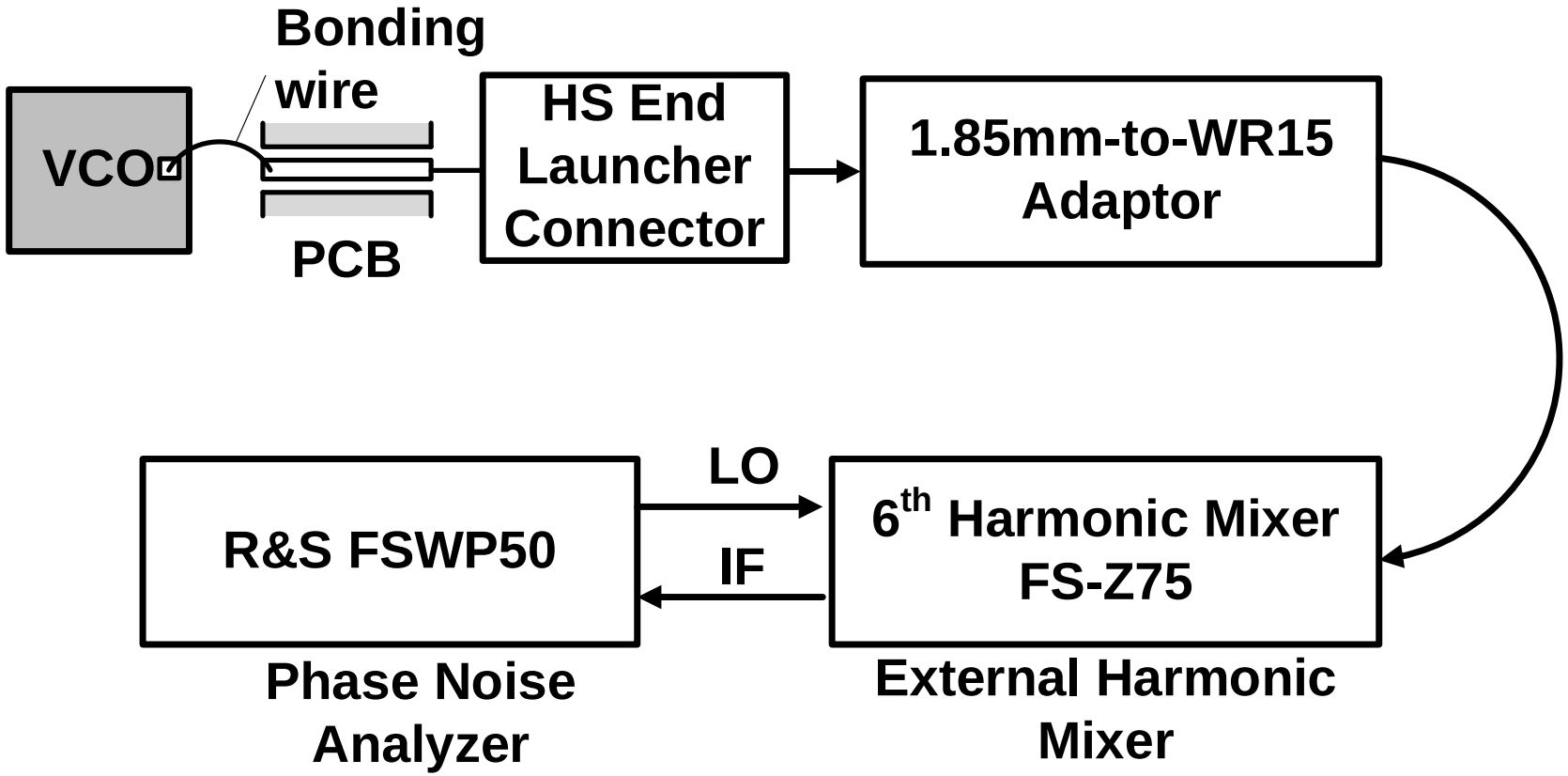
Chip Microphotograph



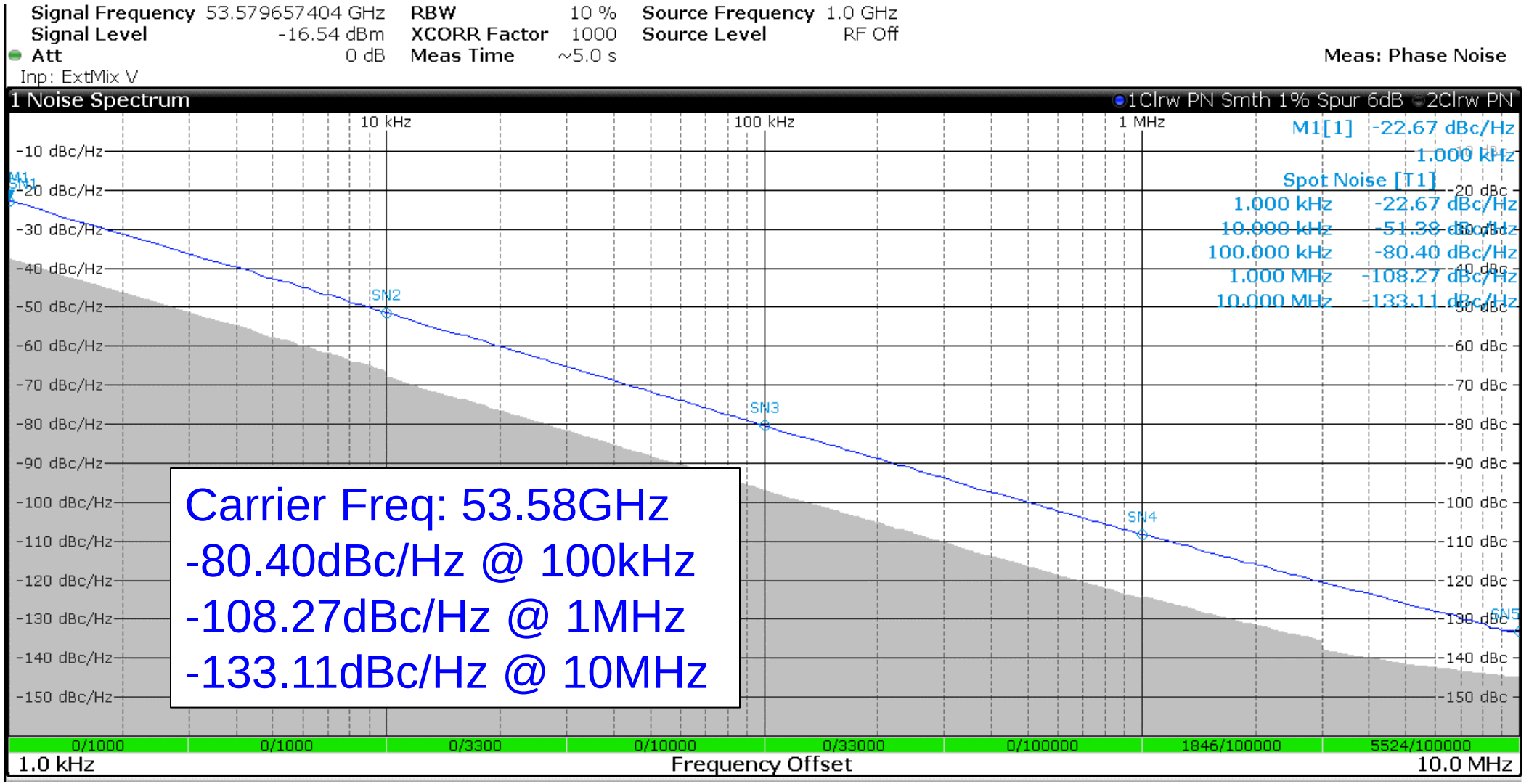
- 65nm CMOS Process
- Core area: 0.15mm^2
- Supply voltage: 0.65V
- Power consumption: 107~125mW

Measurement Setup

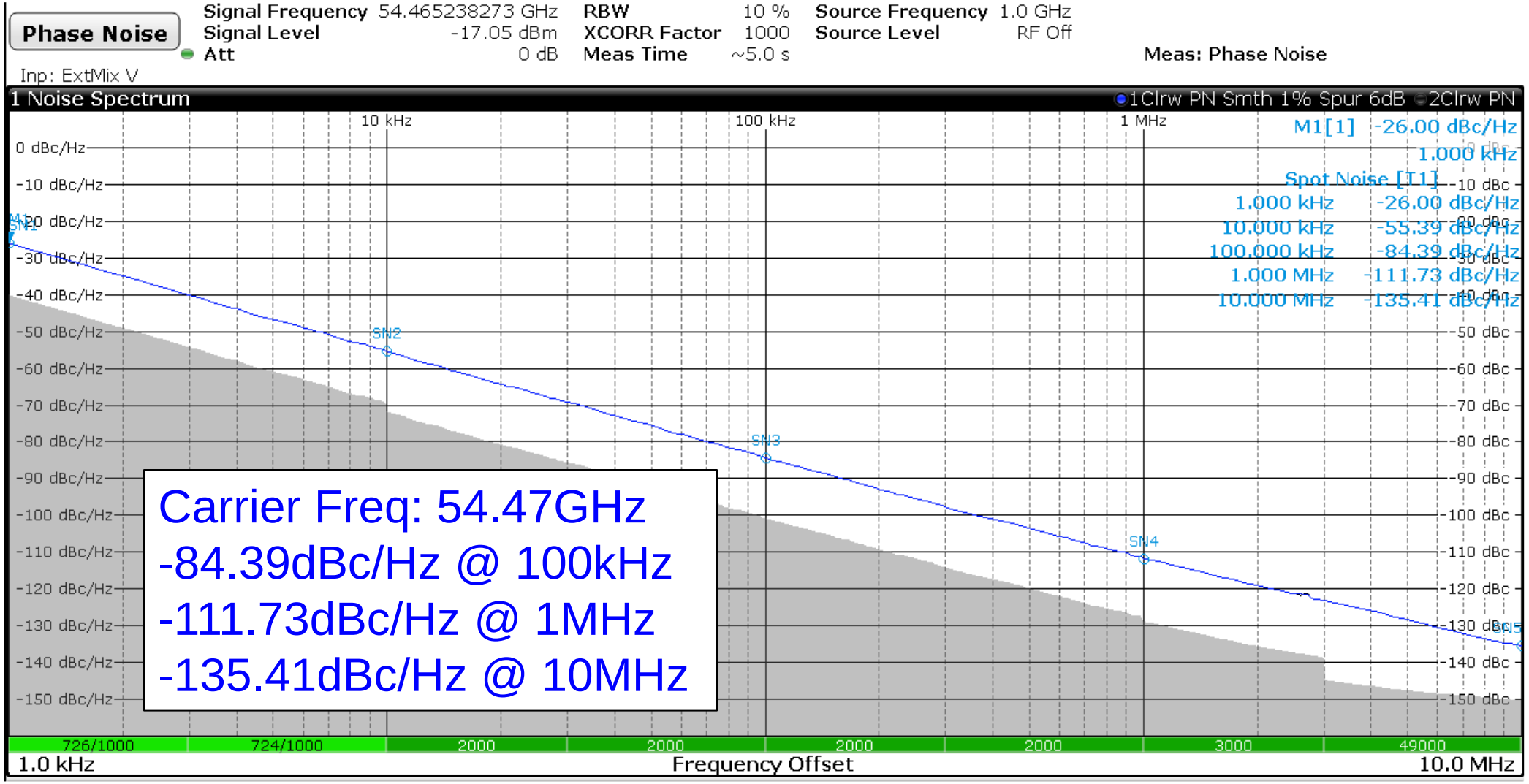
- One-time cap-bank calibration is performed manually
- After-that, all cap-bank codes are identically tuned



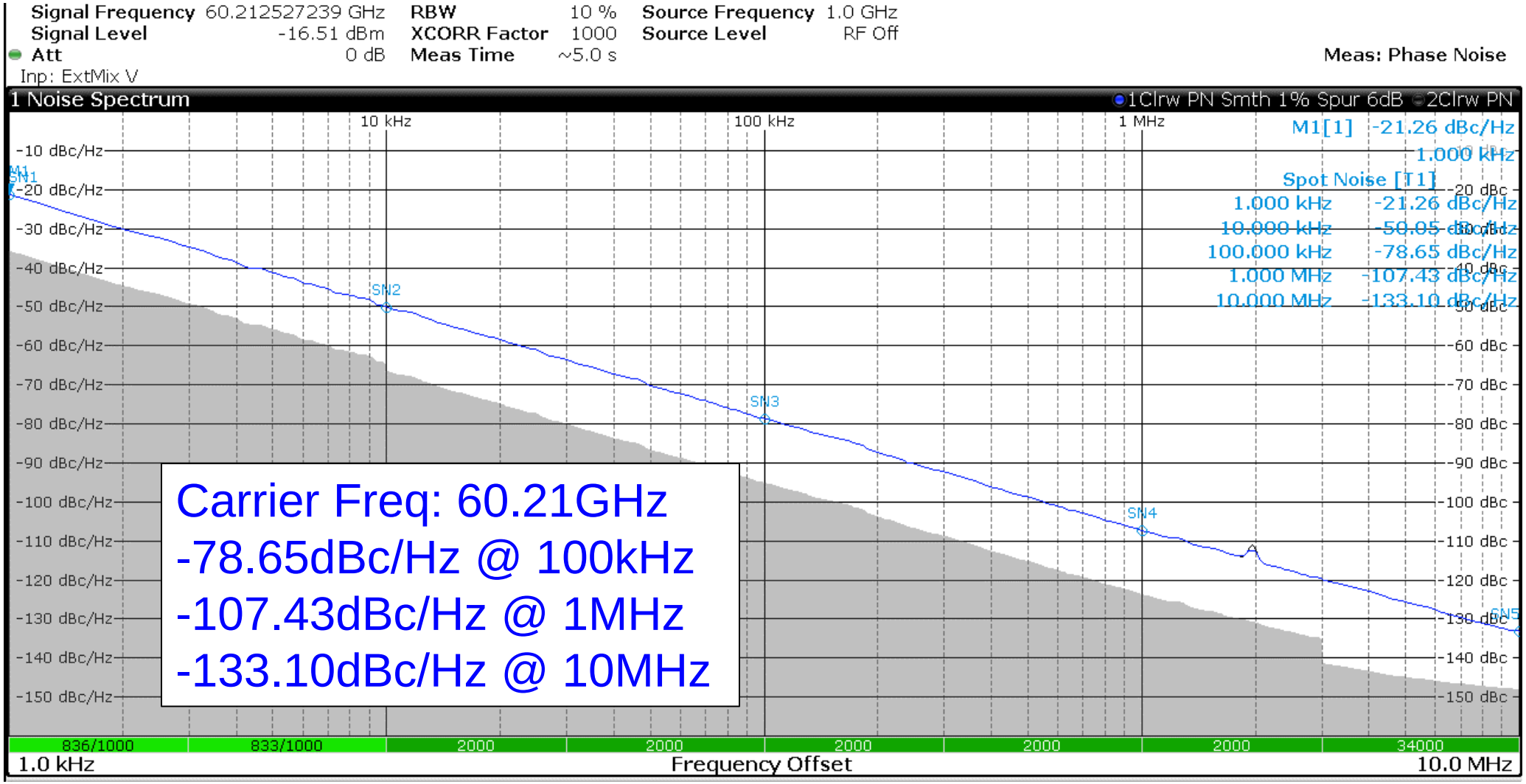
Measured Phase Noise Plot



Measured Phase Noise Plot

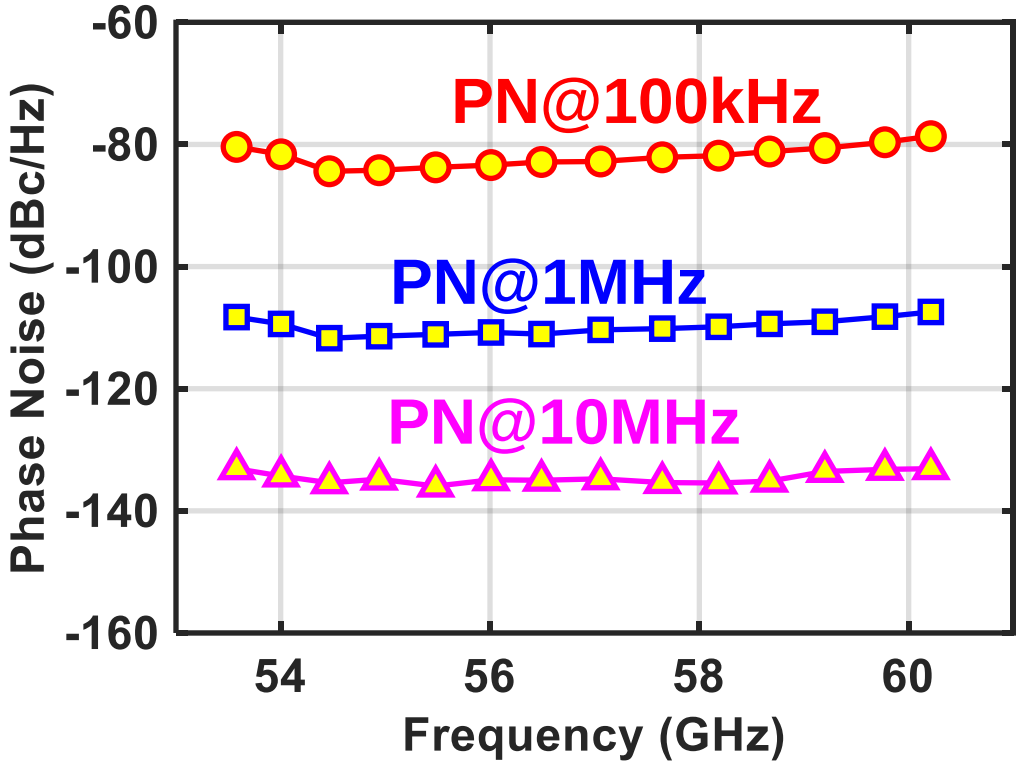


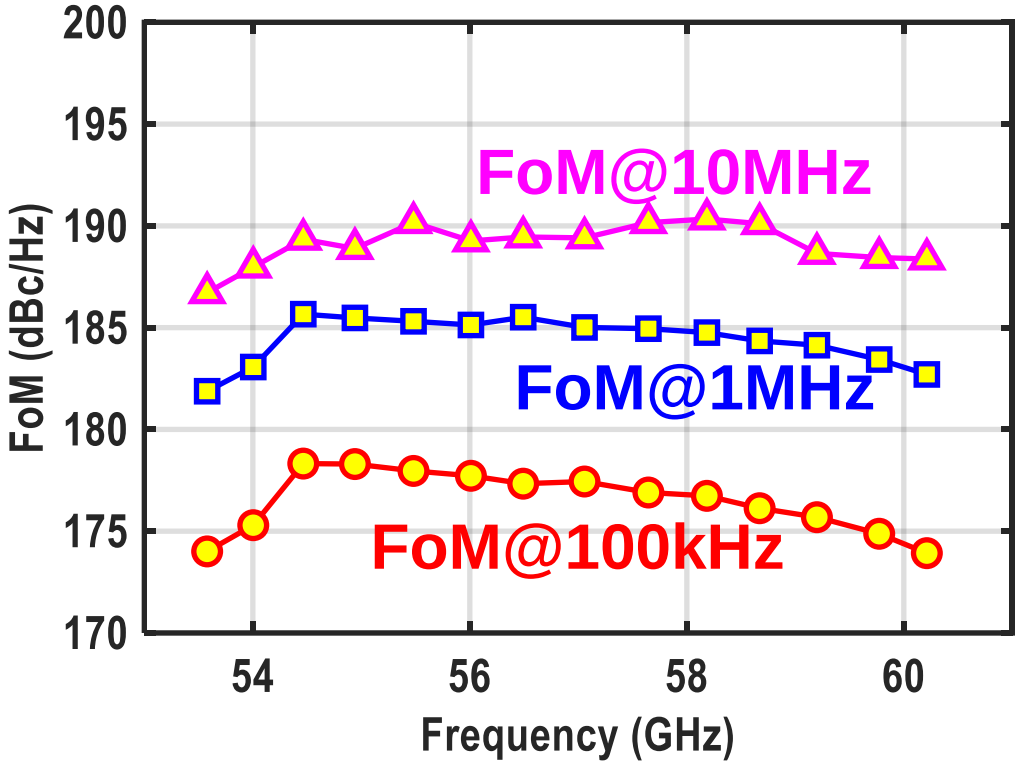
Measured Phase Noise Plot



Carrier Freq: 60.21GHz
-78.65dBc/Hz @ 100kHz
-107.43dBc/Hz @ 1MHz
-133.10dBc/Hz @ 10MHz

Measured Phase Noise and FoM





- PN@1MHz: -111.7~-107.4 dBc/Hz
- PN@10MHz: -136.0~-133.1 dBc/Hz

- **FoM@1MHz: 181.9~185.7 dBc/Hz**
- **FoM@10MHz: 186.7~190.3 dBc/Hz**

Performance Comparison

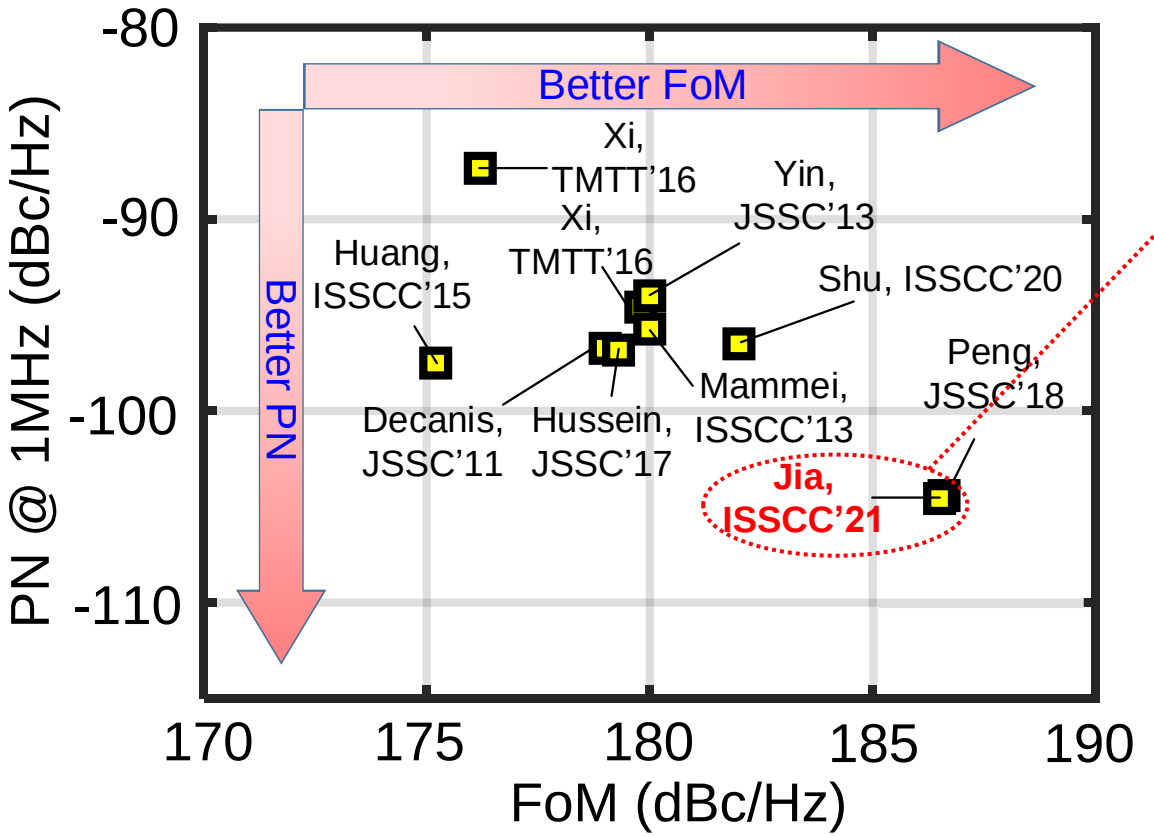
- **Compared with recent mm-wave fundamental VCOs**

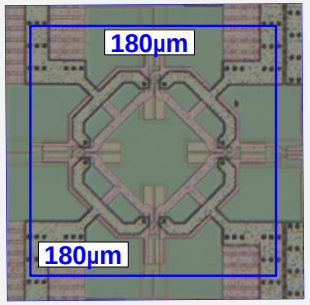
		This work	JSSC'18 [4]	ISSCC'20 [5]	ISSCC'21 [6]	TMTT'16 [7]	JSSC'11 [8]
Technology		**65nm CMOS**	65nm CMOS	40nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
No. of Cores		**16**	4	4	4	2	2
Tuning range (GHz)		**53.6 to 60.2**	42.9 to 50.6	18.6 to 40.1	52.4 to 60.4	51.7 to 56.6	56 to 60.4
Supply Voltage (V)		**0.65**	0.9	1.1	0.55	1.0	1
Power (mW)		**107 to 125**	20.9 to 21.5	9 to 15	22.5 to 23.6	24	22
Phase Noise (dBc/Hz)	**100kHz**	**-84.4 to -78.7**	-75*	-72.7 to -82.3	-75.2 to -71.2	N/A	-67*
	1MHz	**-111.7 to -107.4**	-106.1 to -101.6**	-108.5 to -100.3	-104.7 to -101.4	-95	-97 to -95
	10MHz	**-136.0 to -133.1**	-121*	-130.3 to -122.7	N/A	-119.2	-117
FoM (dBc/Hz)	**100kHz**	**173.9 to 178.3**	N/A	N/A	172.1 to 176.9	N/A	N/A
	1MHz	**181.9 to 185.7**	181.1 to 186.6**	181.4 to 184.4	182.2 to 186.5	179.8	177 to 179
	10MHz	**186.7 to 190.3**	N/A	183.0 to 186.3	N/A	N/A	N/A
Core Area (mm2)		**0.15**	0.039	0.08	0.032	0.032	0.075

*Estimated from figures **Normalized from 3MHz offset FoM=$|PN|+20\log_{10}(f_0/\Delta f)-10\log10(P_{DC}/1mW)$

Performance Comparison

- **Compared with recent mm-wave fundamental VCOs**



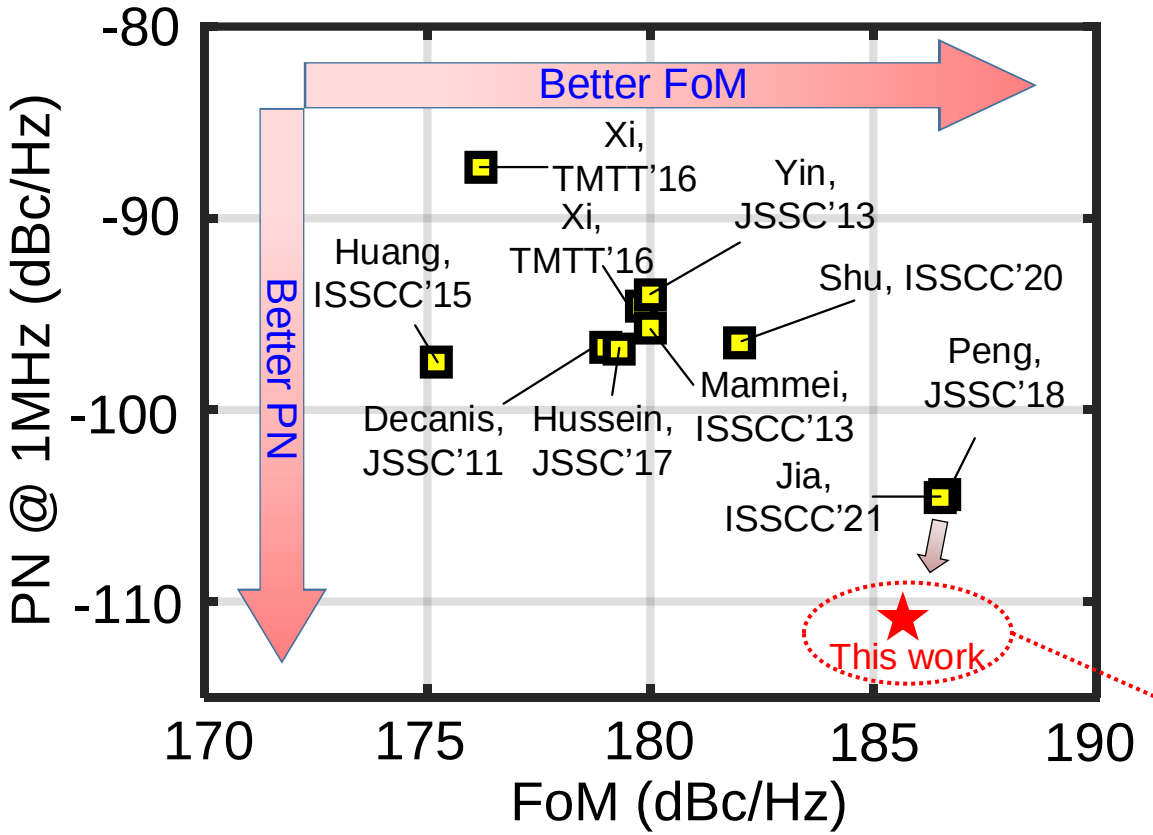


circulator-topology quad-core oscillator

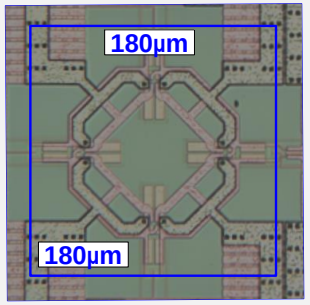
Phase noise in the figure is normalized to 60GHz

Performance Comparison

- **Compared with recent mm-wave fundamental VCOs**

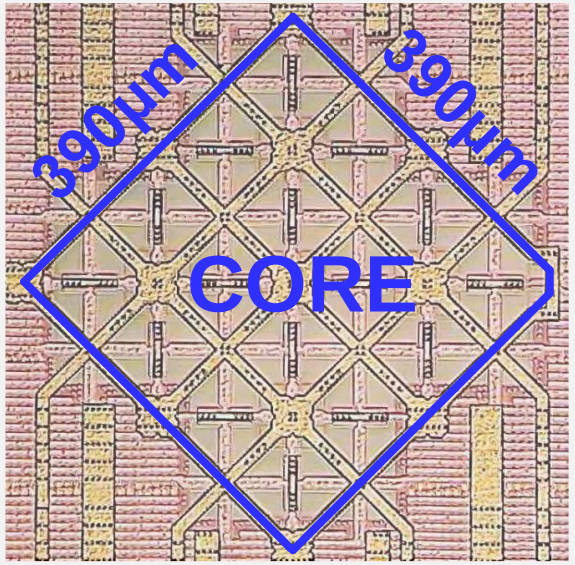


Phase noise in the figure is normalized to 60GHz



circulator-topology
quad-core oscillator

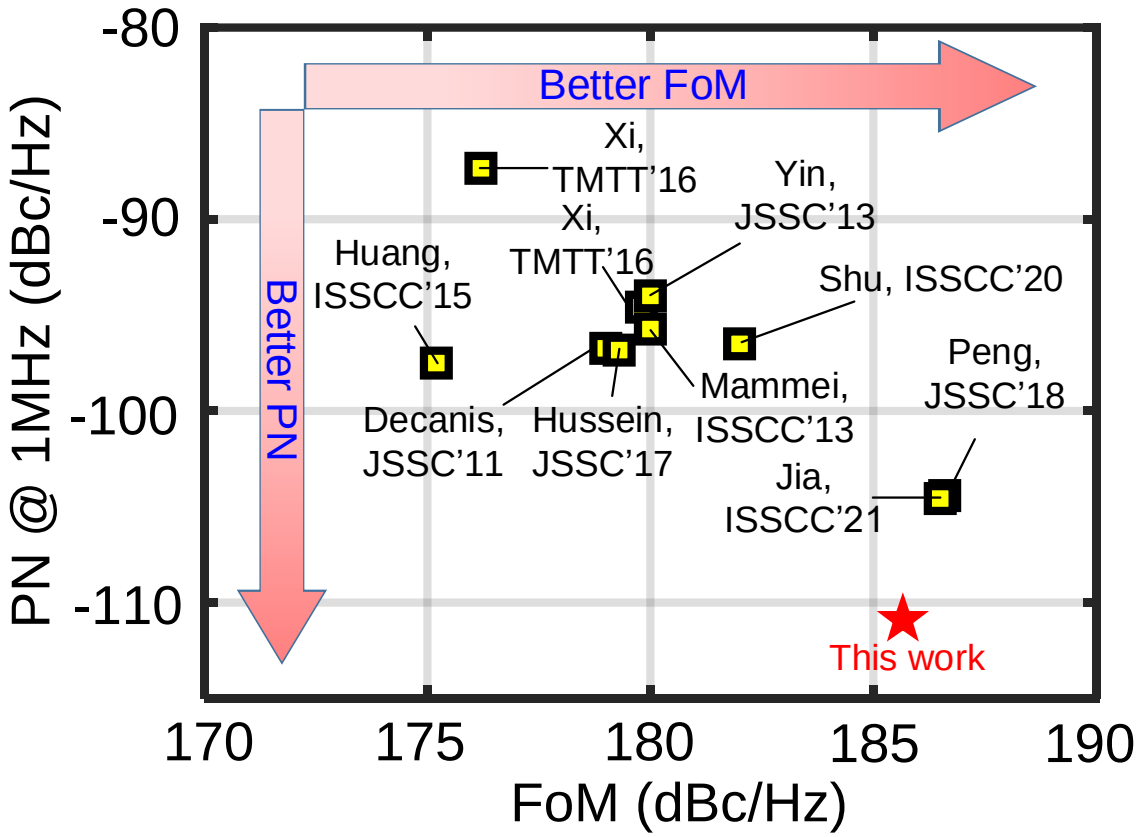
7.0dB PN improvement
0.8dB FoM degradation

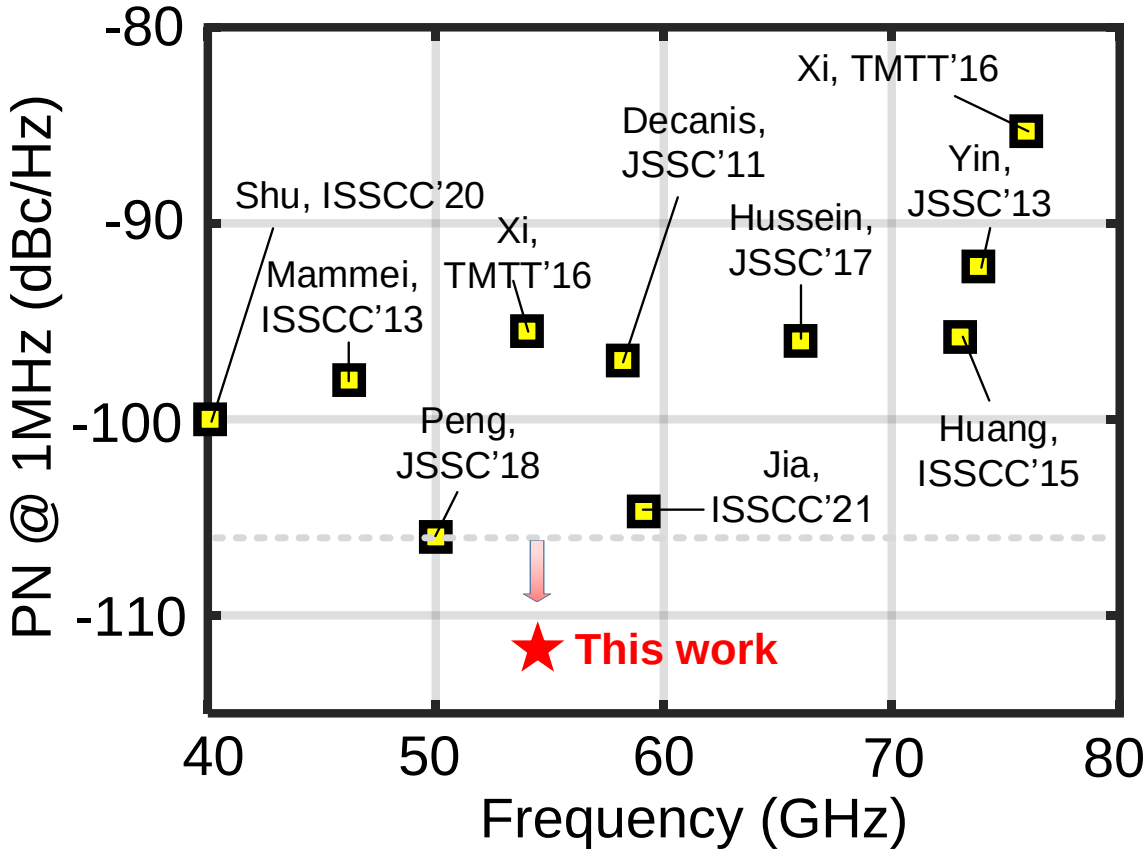


mesh-topology
16-core oscillator

Performance Comparison

- **Compared with recent mm-wave fundamental VCOs**





Phase noise in the figure is normalized to 60GHz

Conclusions

- Two small Rp approaches for high-performance
  - Series-resonance architecture
  - Multi-core architecture
- Two technologies enable many-core oscillator
  - Mode-rejection-coupled synchronization
  - Mesh-topology floorplan
- 16-core oscillator prototype in 65nm CMOS
  - -111.7dBc/Hz at 1MHz from 54.47GHz
  - 190.3dBc/Hz FoM at 10MHz offset

Q & A

Thank you for your attentions!