An Event-Driven Pipelined ADC with 100x BW Scaling Using A 3-Stage Cascoded Floating Inverter Amplifier

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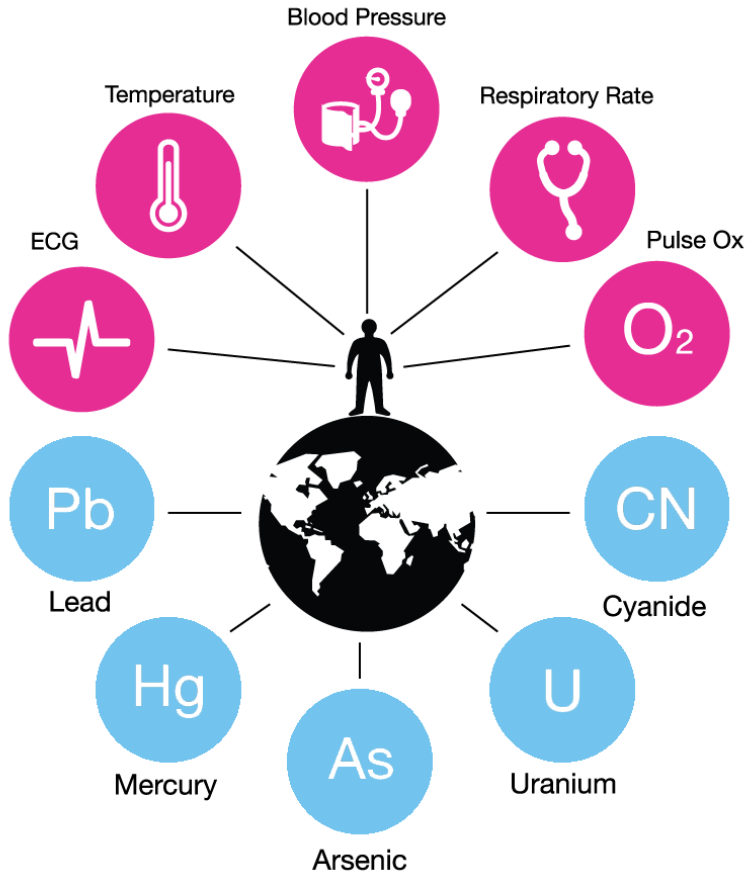
Outline

- Motivation
- Proposed Cascoded Floating Inverter Amplifier (FIA)
- Pipelined SAR Circuit Implementation
- Measurement Results
- Conclusion

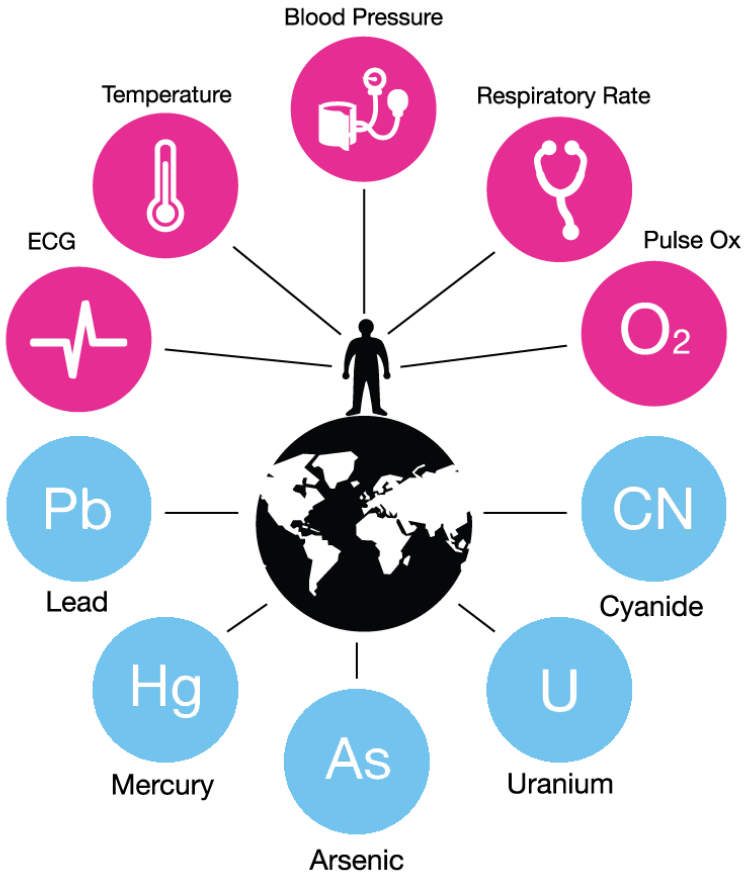
Event-Driven ADC

- Multi-standard wireless
- IoT with sparse signals



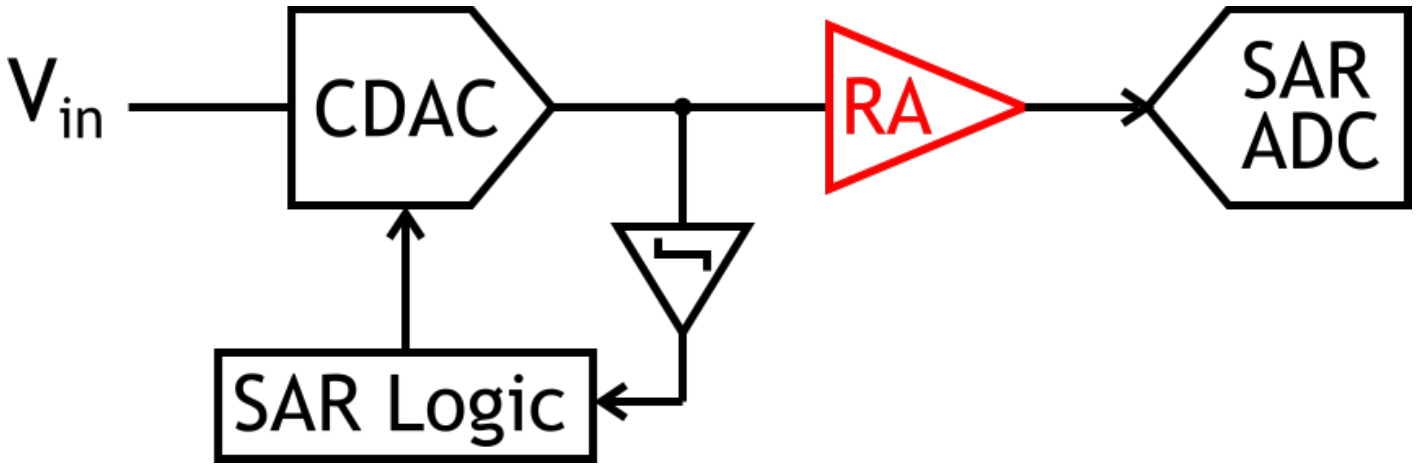
Event-Driven ADC

- Multi-standard wireless
- IoT with sparse signals
  - ➔Scalable power w.r.t. signal rates
  - ➔Duty-cycling friendly



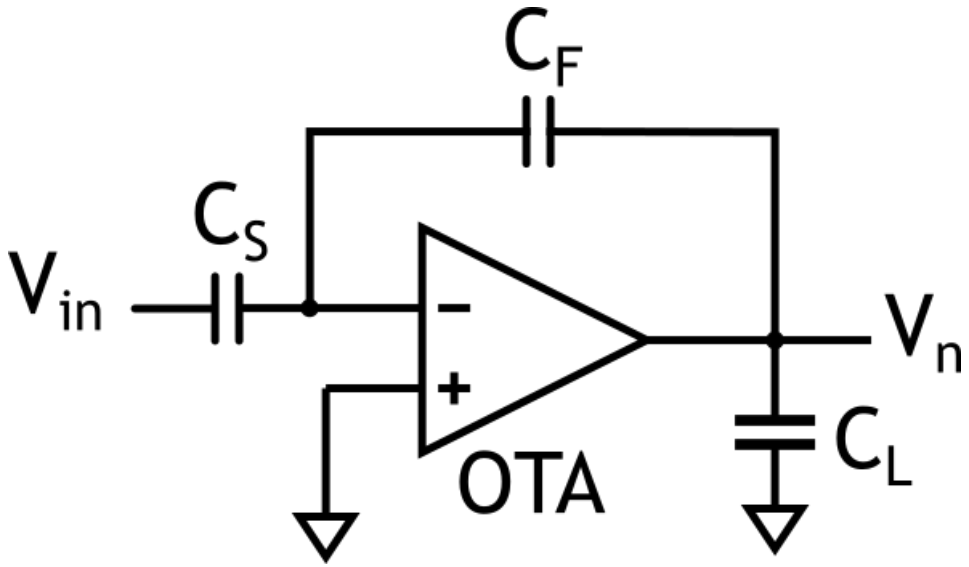
Event-Driven ADC

- **Pipelined SAR ADC**
  - **High speed**
  - **High precision**
- **Residue amplification is the *key* operation!**



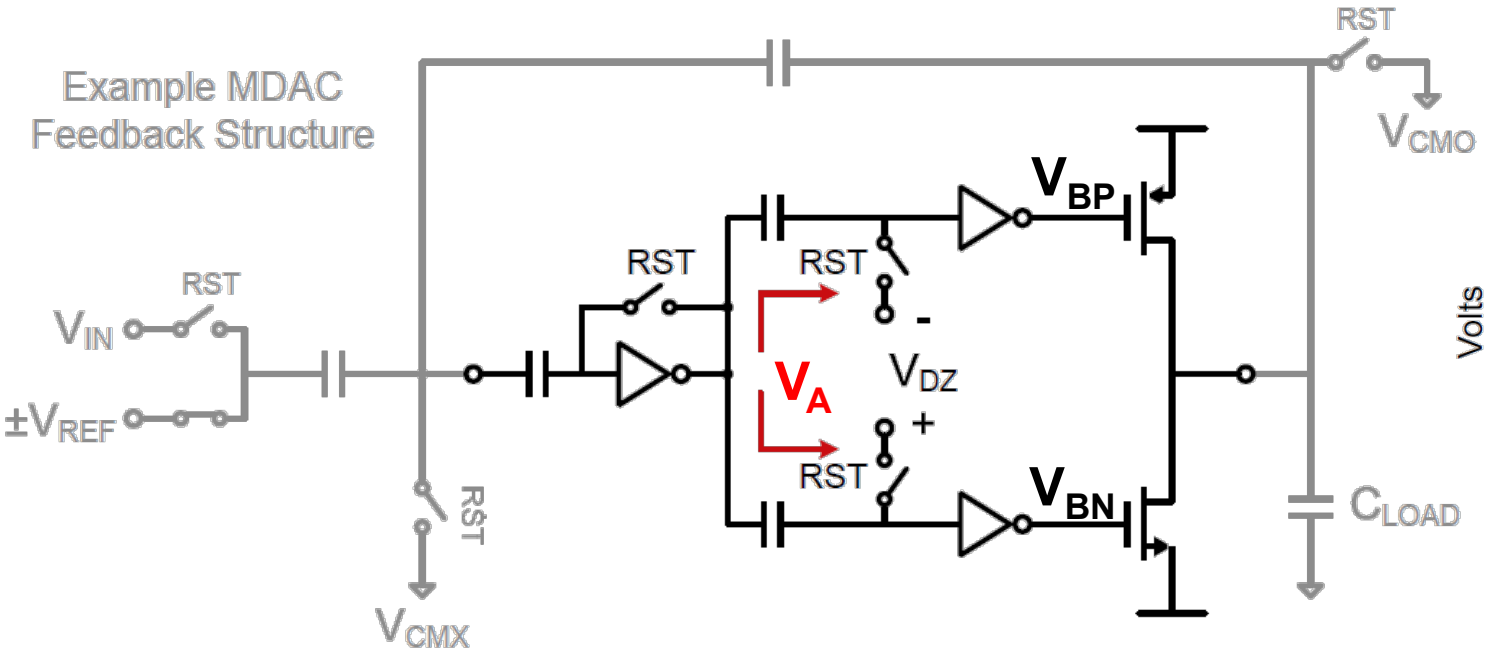
Residue Amplification

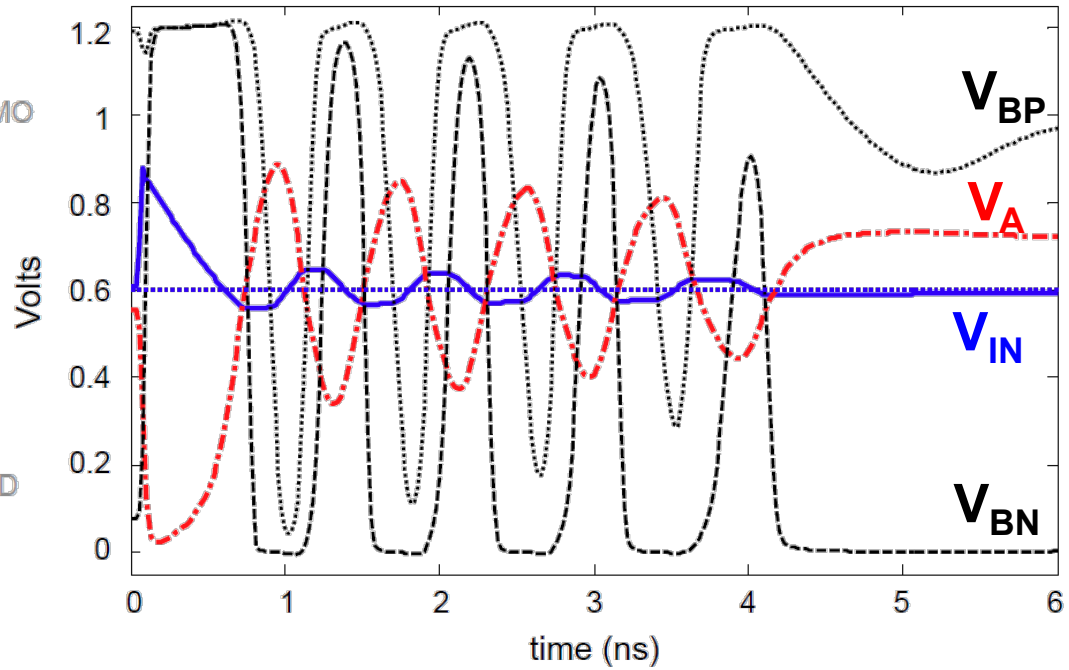
- **Closed-loop OTA**
  - **–High gain ☺**
  - **–PVT-robust stability ☺**
  - **–Not suitable for duty-cycling ☹**



Residue Amplification

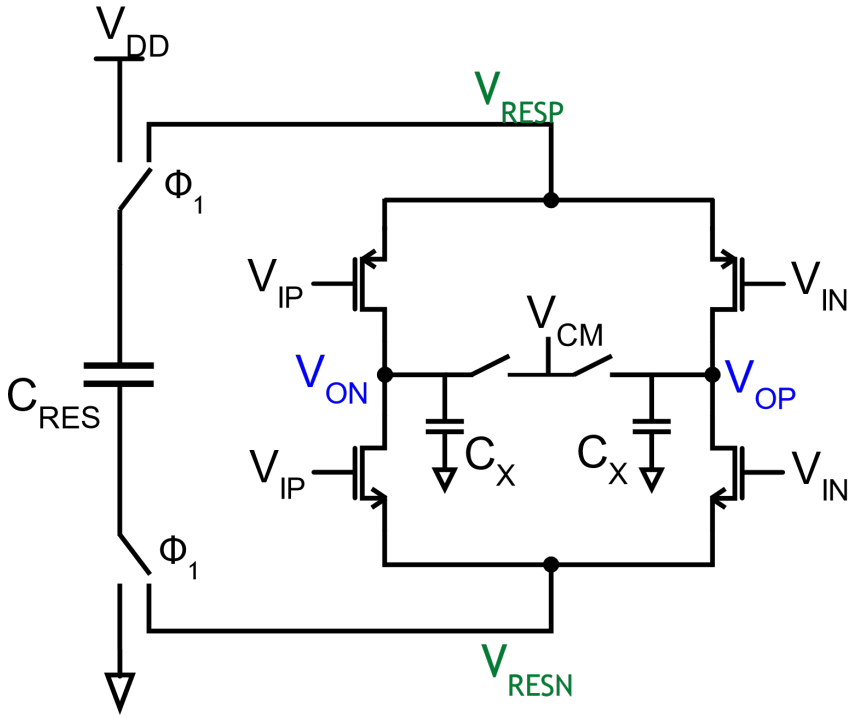
- **Closed-loop Ring Amp [Hershberg, JSSC '12]**
  - **Duty-cycling friendly ☺**
  - **PVT sensitive dead-zone biasing ☹**
  - **Constant 1st-stage dominant power ☹**

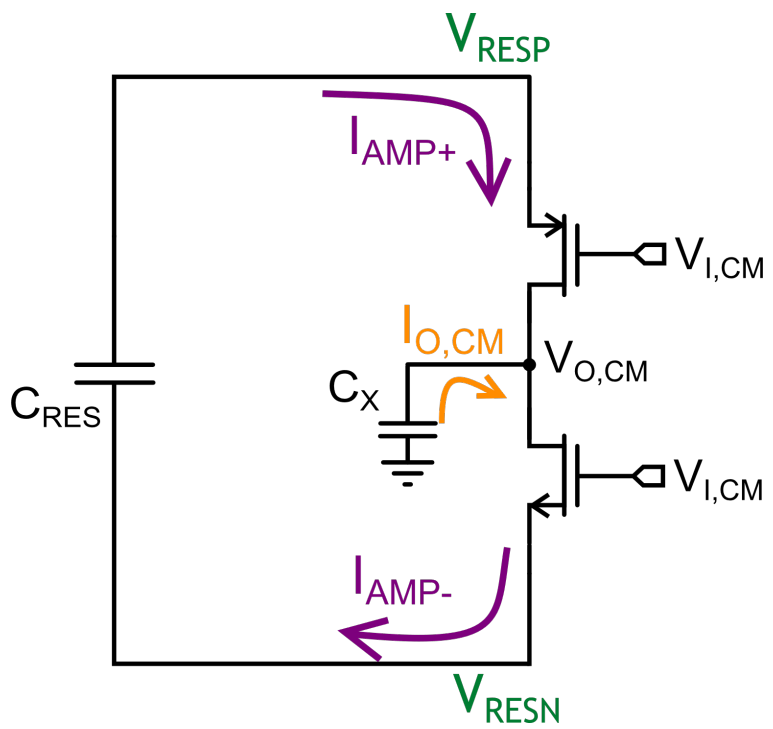




Residue Amplification

- Floating Inverter Amplifier (FIA) [Tang, VLSI '19]
  - Current reuse ☺
  - Intrinsic CMFB ☺

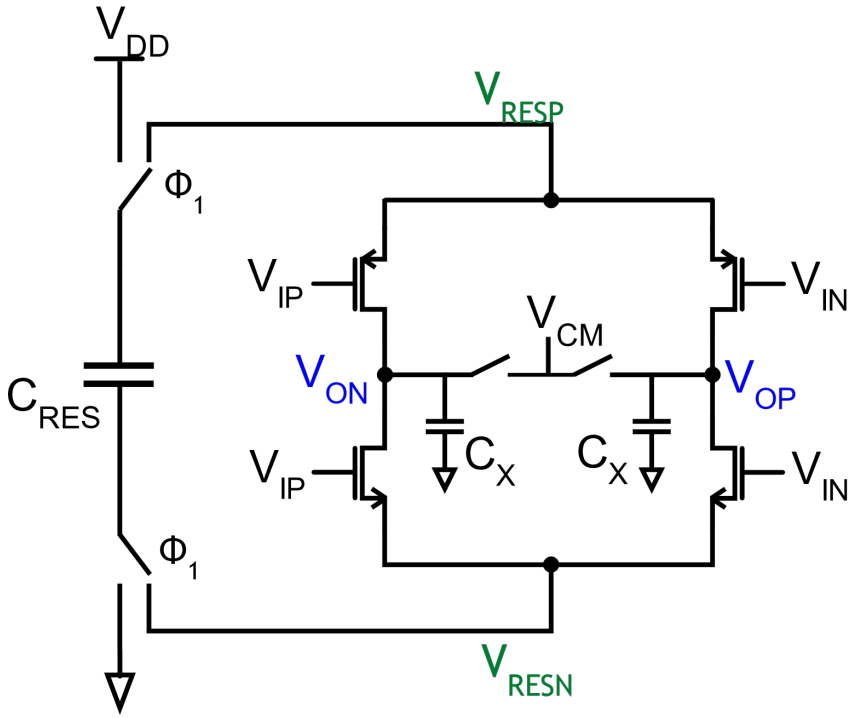


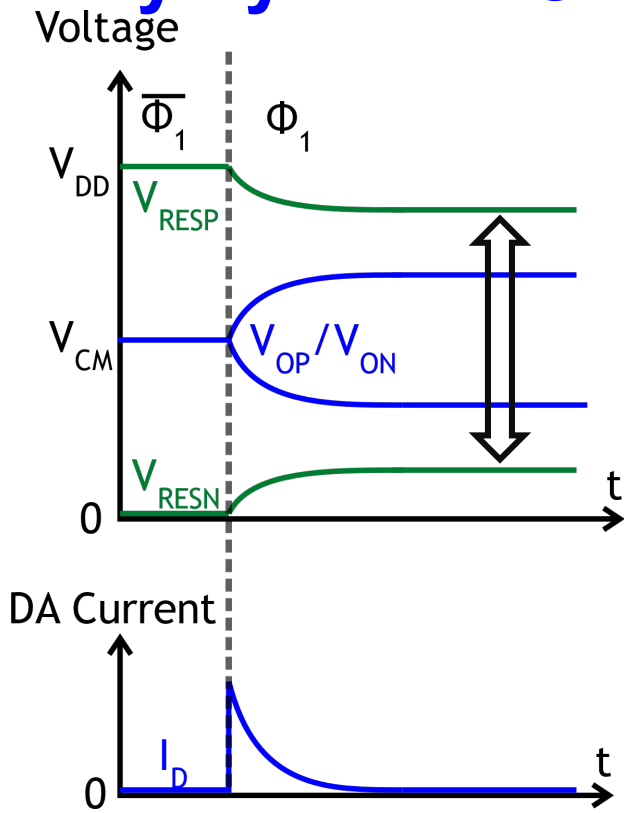


Common-mode equivalent

Residue Amplification

- Floating Inverter Amplifier (FIA) [Tang, VLSI '19]
  - Current reuse ☺
  - Intrinsic CMFB ☺
  - Self-quenching ☺
  - Fully dynamic ☺

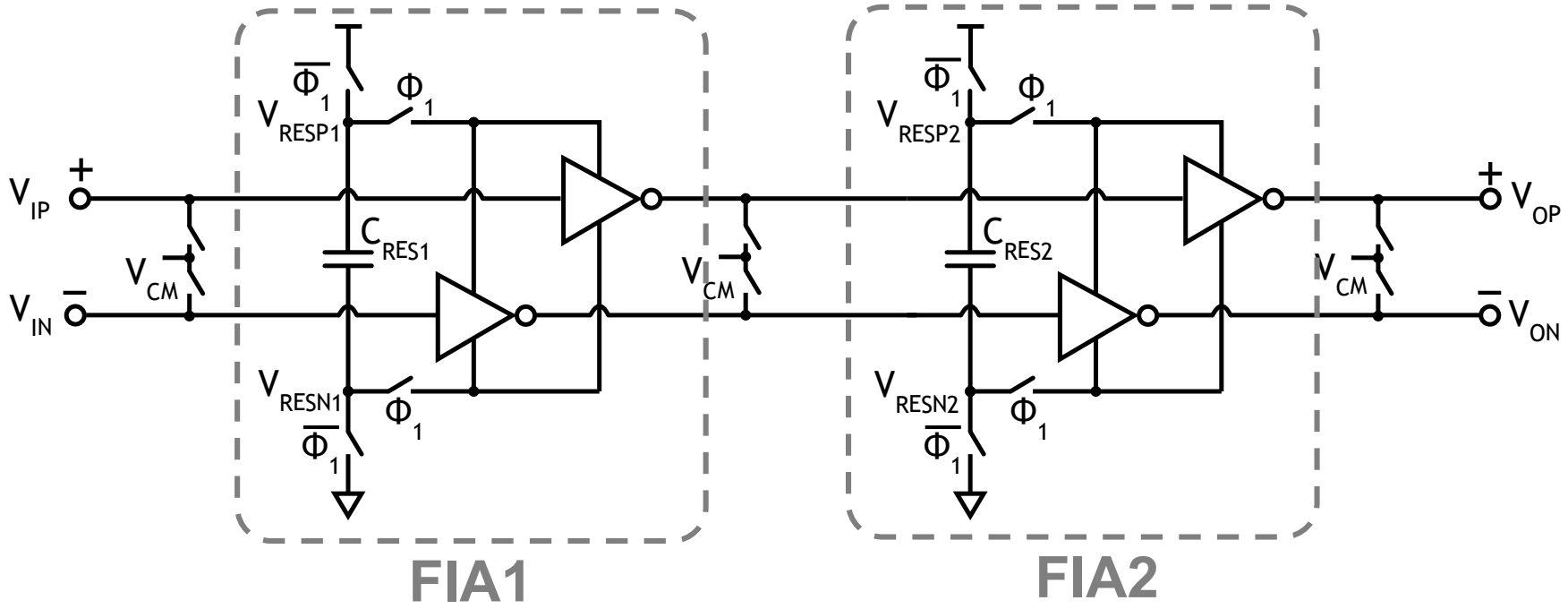




Self-quenched
$V_{RES}<V_{THP}+V_{THN}$

Residue Amplification

- **Closed-loop FIA [Tang, ISSCC ’20]**
  - –Duty-cycling friendly ☺
  - –Time-decaying power ☺
  - –PVT-robust stability ☺
  - –Moderate gain (33dB) ☹
  - –Low speed ☹



Reside Amplification

Requirements	OTA	Ring-Amp	2-stage FIA	Proposed 3-stage cascoded FIA
High gain	☺	☺	☹	☺
High speed	☺	☺	☹	☺
Loop stability	☺	😐	☺	☺
Duty cycling	☹	☺	☺	☺
Decaying power	☹	😐	☺	☺

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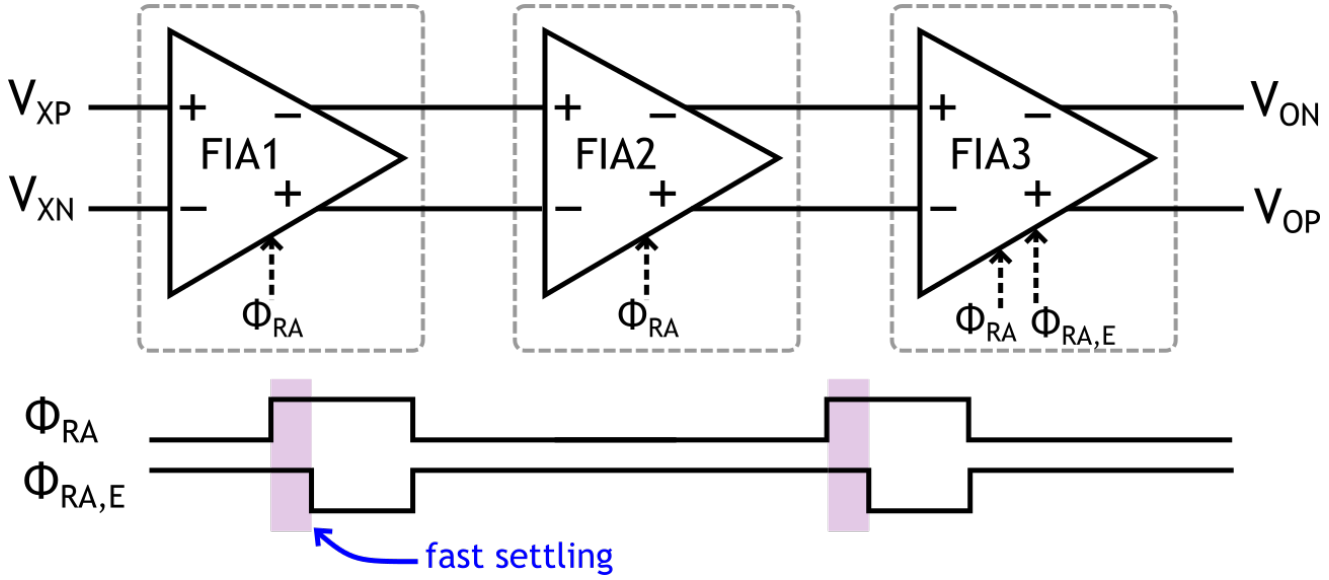
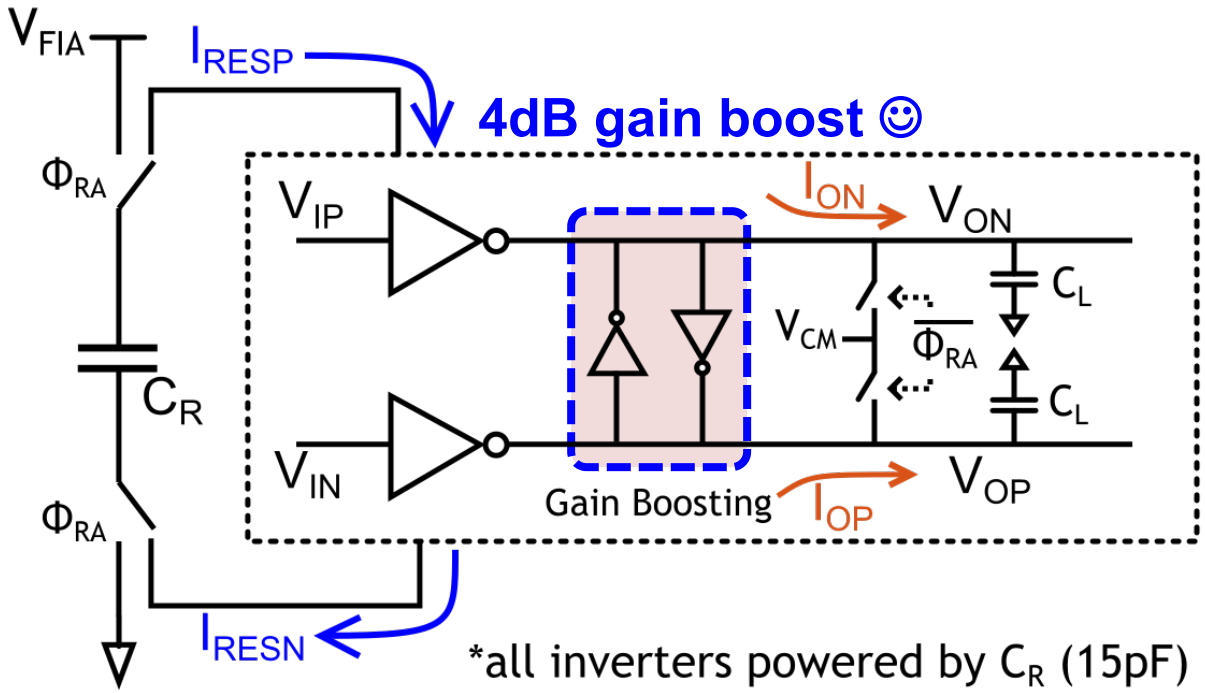
Residue Amplification

- **Proposed 3-stage cascoded FIA**
  - **Gain enhancement: 3-stage + dynamic cascode amplifier**
  - **Speed enhancement: two-step operation**



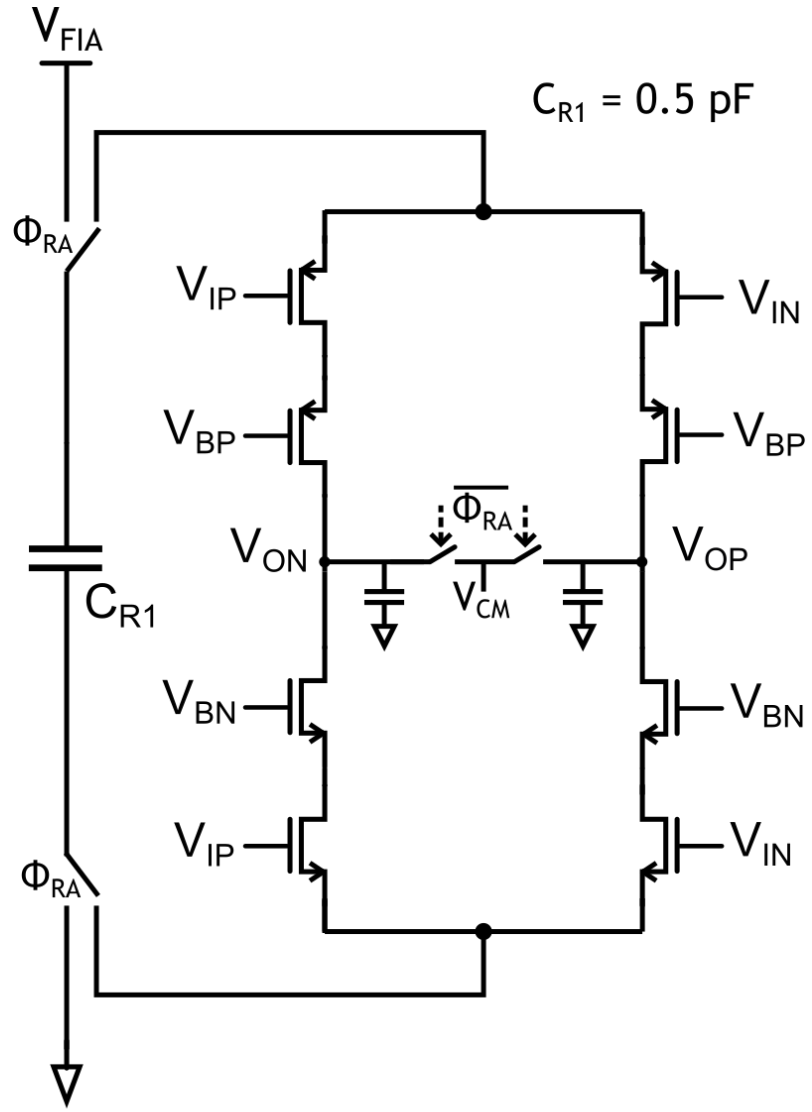
Proposed 3-stage Cascoded FIA

- 1st/2nd-stage FIA
  - –Local gain boosted by negative-R
  - –22dB each stage



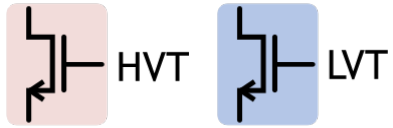
Proposed 3-stage Cascoded FIA

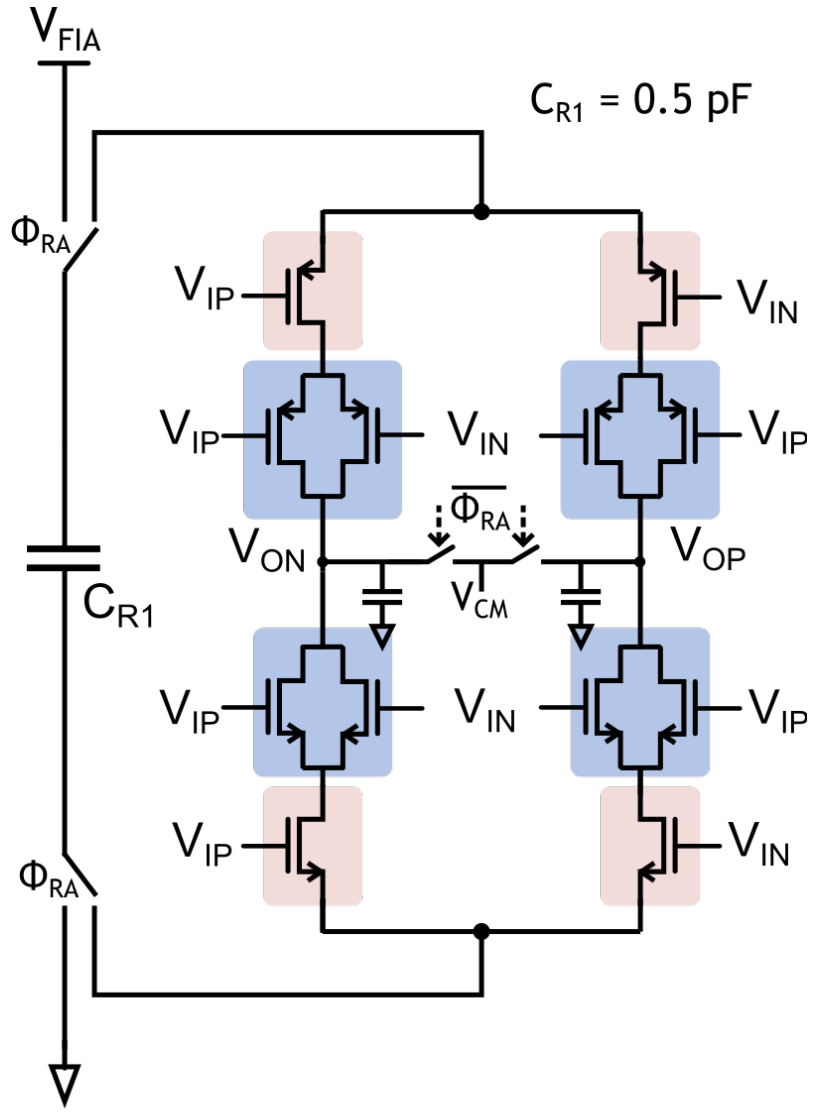
- 3rd-stage cascoded FIA
  - ~40dB gain required
  - Dedicated cascode biasing ☹



Proposed 3-stage Cascoded FIA

- 3rd-stage cascoded FIA
  - –Self-biased dynamic cascode

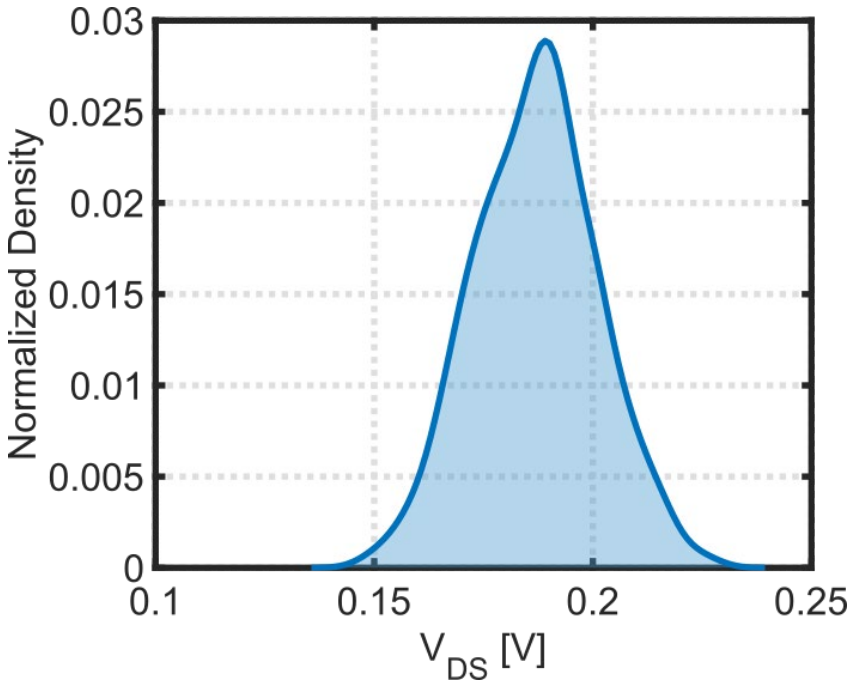


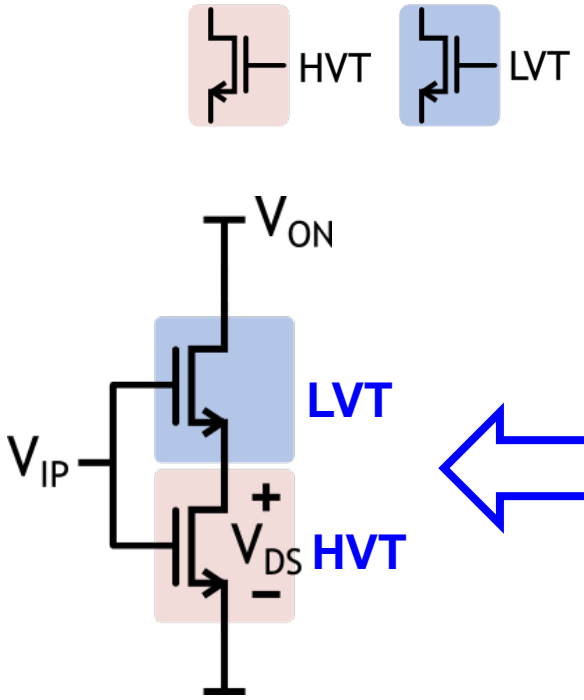


Proposed 3-stage Cascoded FIA

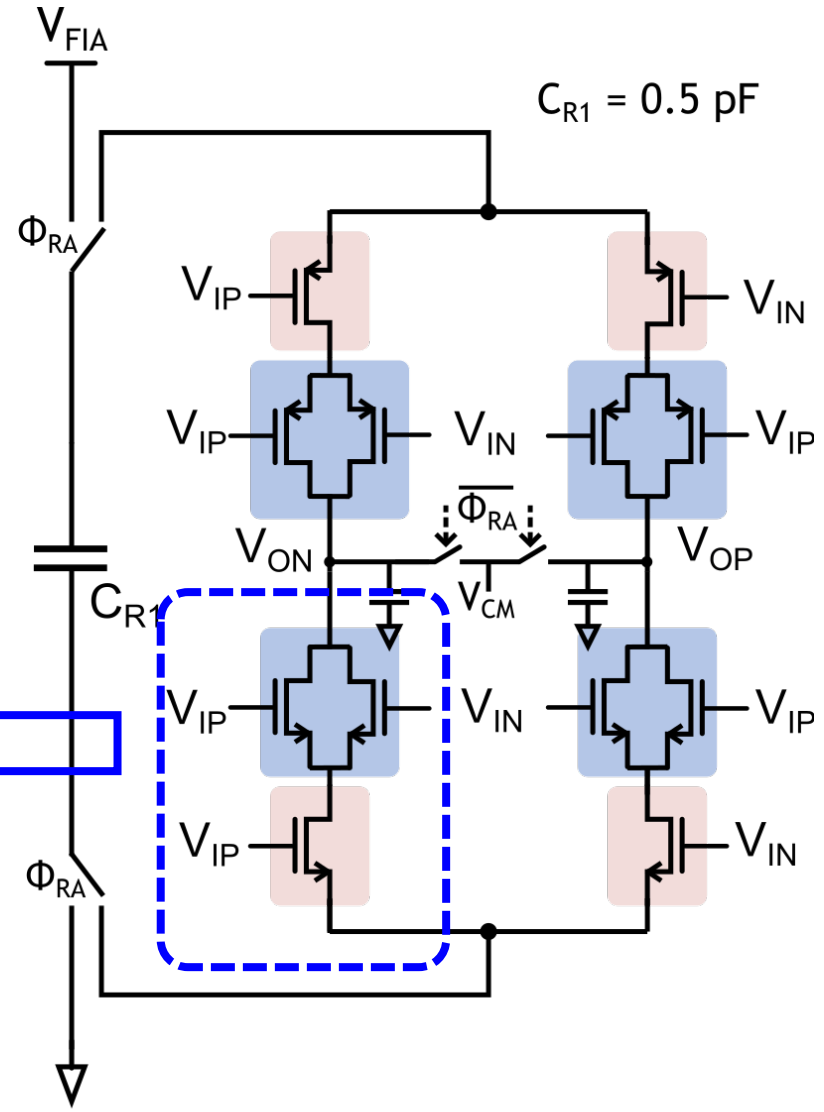
- 3rd-stage cascoded FIA
  - –Self-biased dynamic cascode
  - –38dB DC gain ☺

$$V_{DS} \approx V_{TH,HVT} - V_{TH,LVT}$$



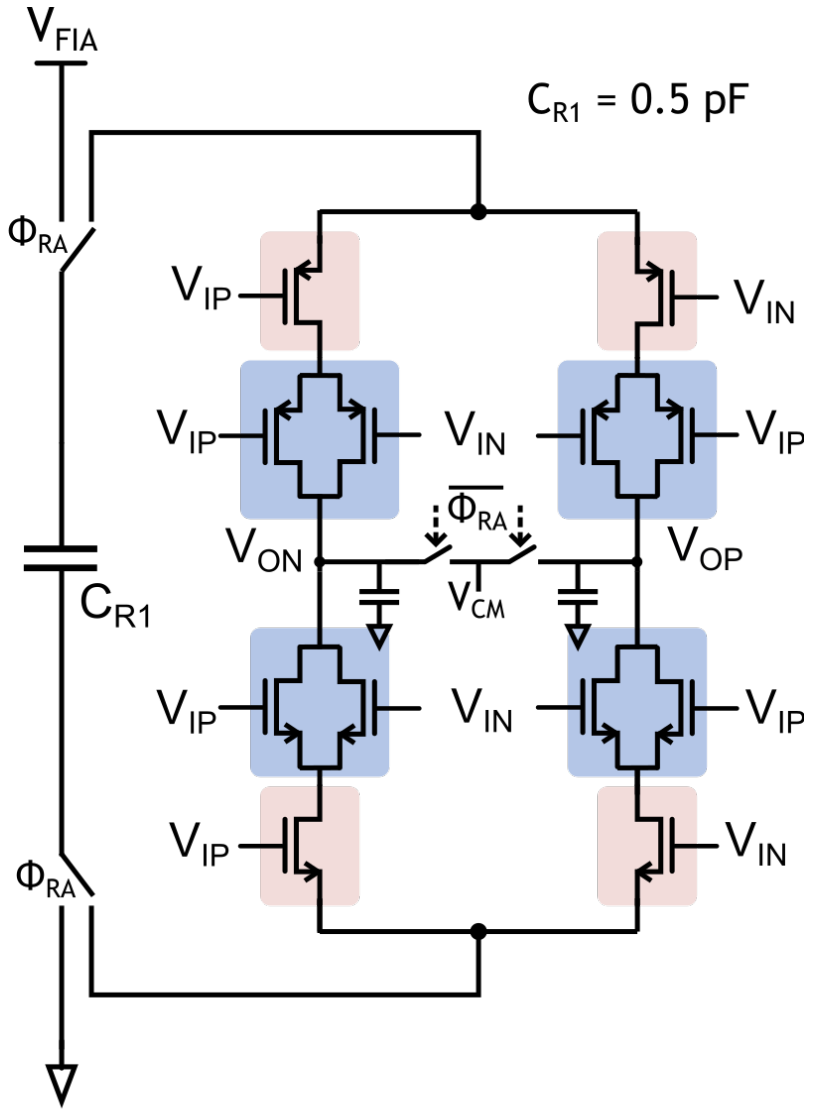


18dB gain boost ☺



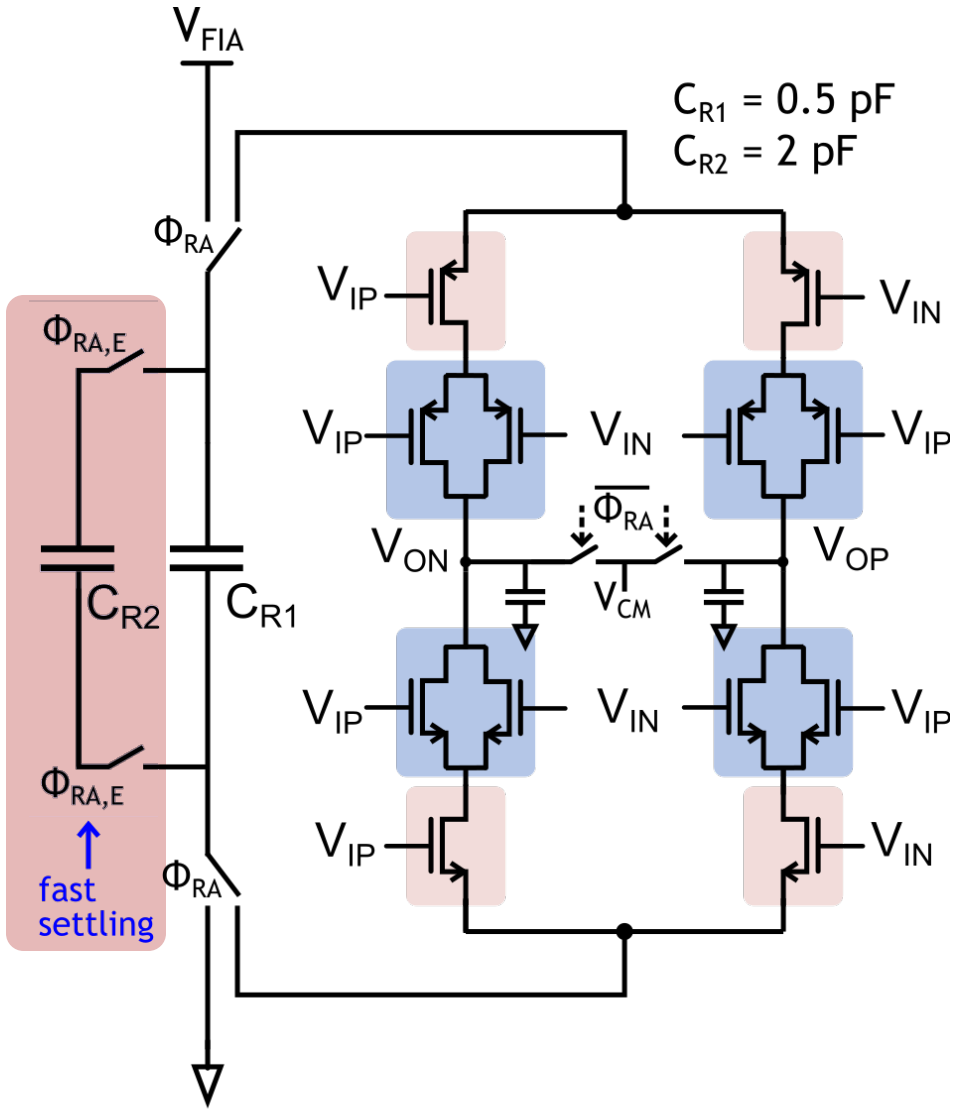
Proposed 3-stage Cascoded FIA

- 3rd-stage cascoded FIA
  - Self-biased dynamic cascode
  - Low speed limited by quenching ☹



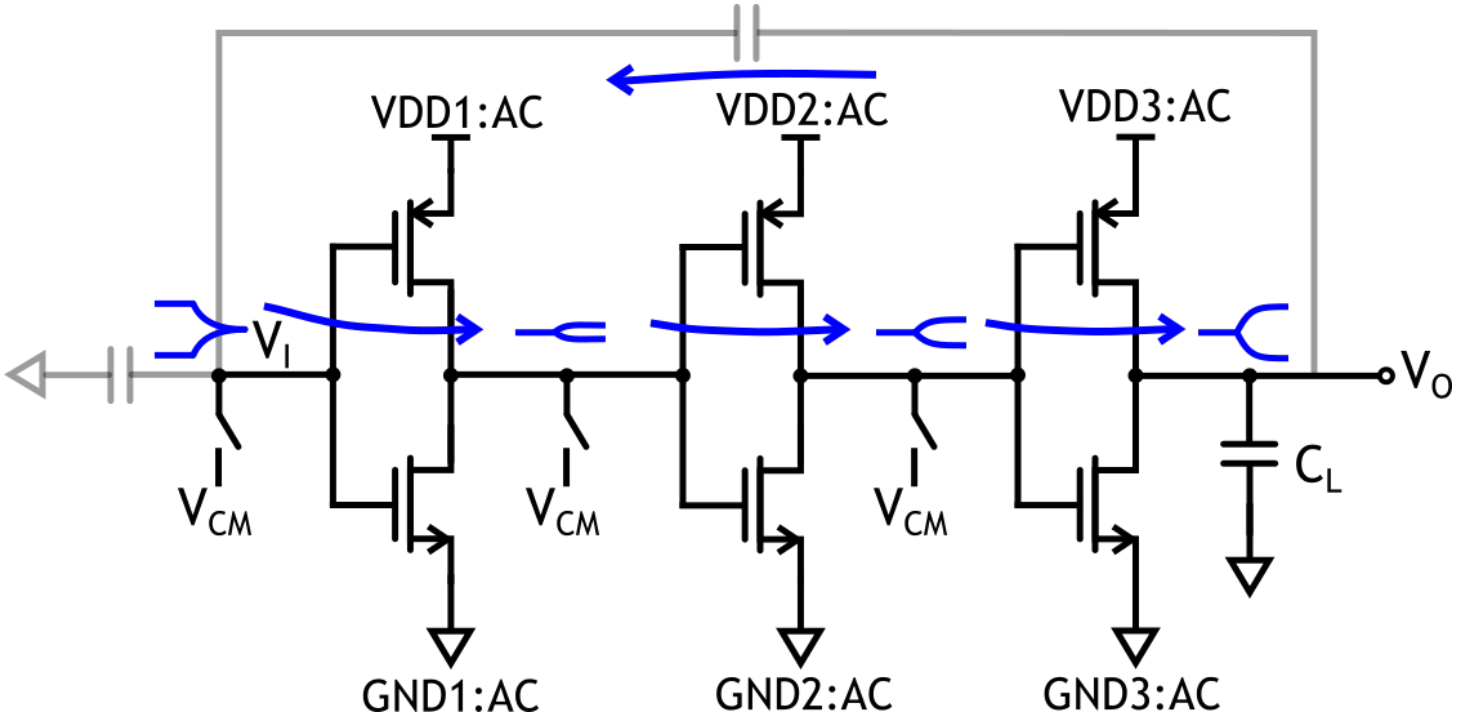
Proposed 3-stage Cascoded FIA

- 3rd-stage cascoded FIA
  - Two-step operation
    - Dual reservoir capacitors for fast settling
    - Single capacitor for fast quenching



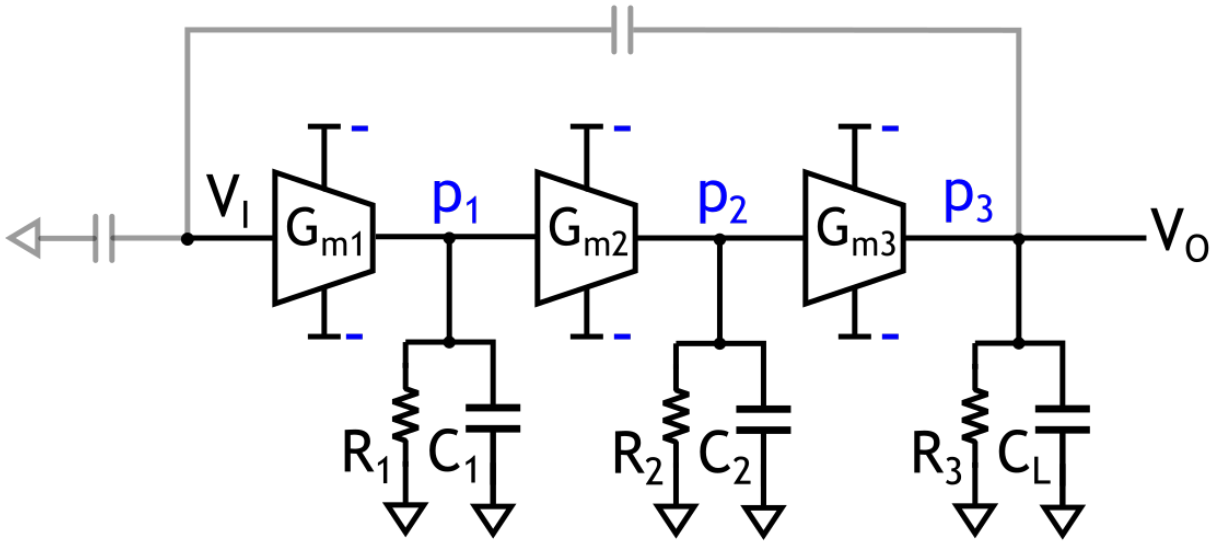
Proposed 3-stage Cascoded FIA

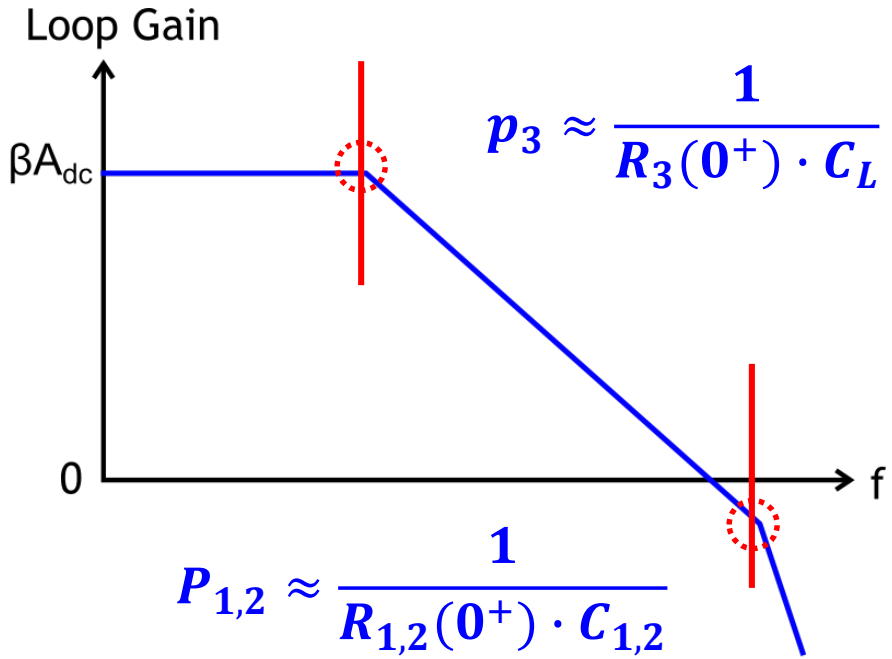
- **Closed-loop 3-stage FIA design**
  - **–82dB DC gain**



Proposed 3-stage Cascoded FIA

- **Closed-loop 3-stage FIA design**
  - **R_3: boosted by cascode stage**
  - **C_L: 2nd-stage SAR DAC**





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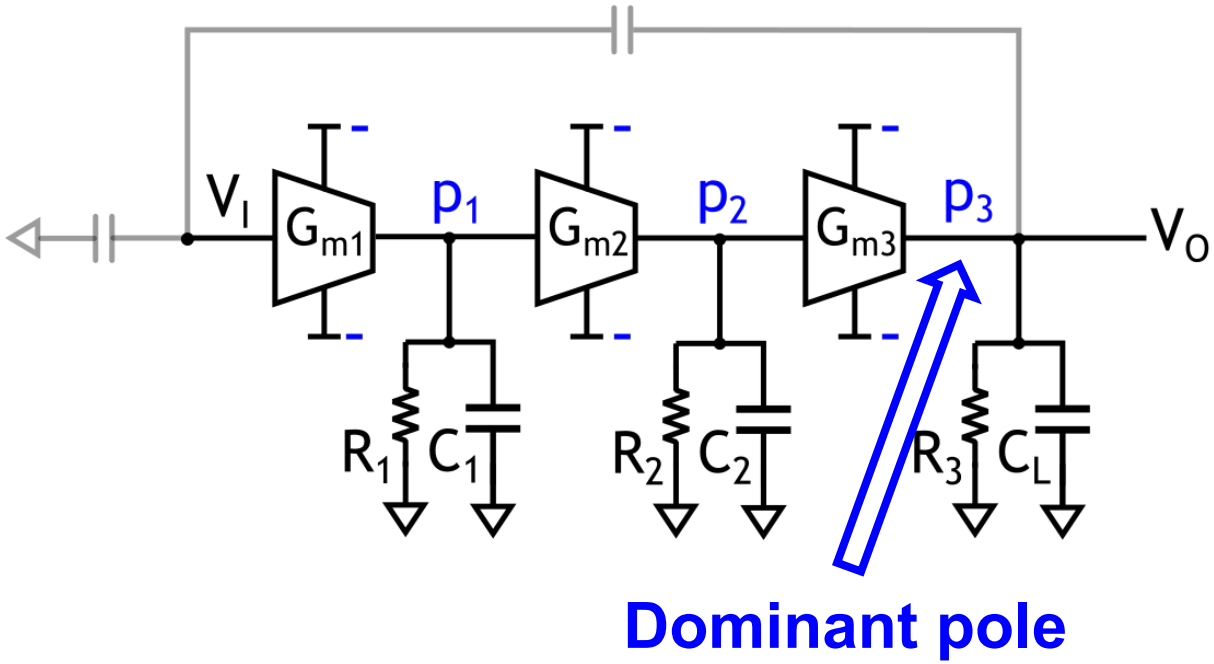
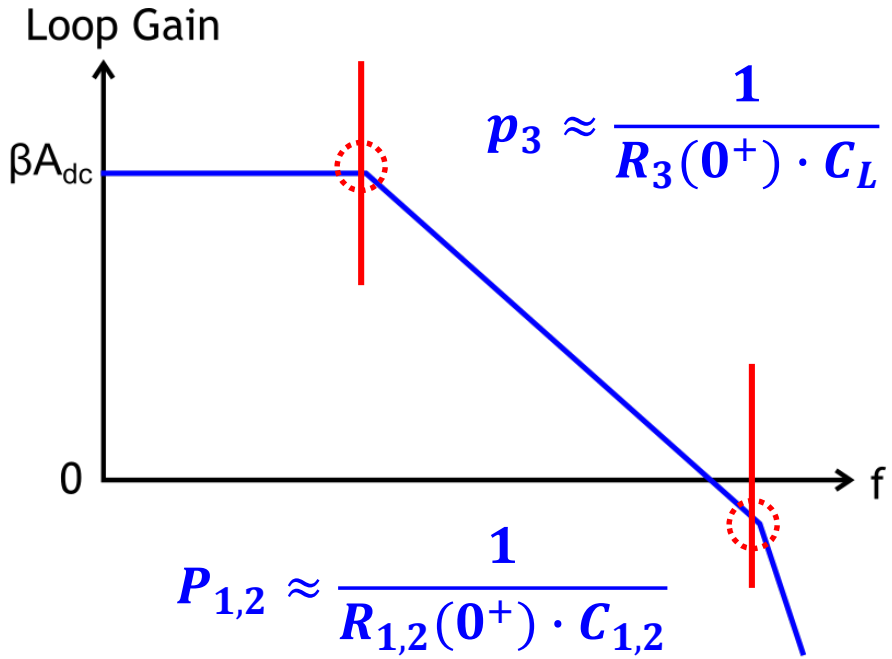
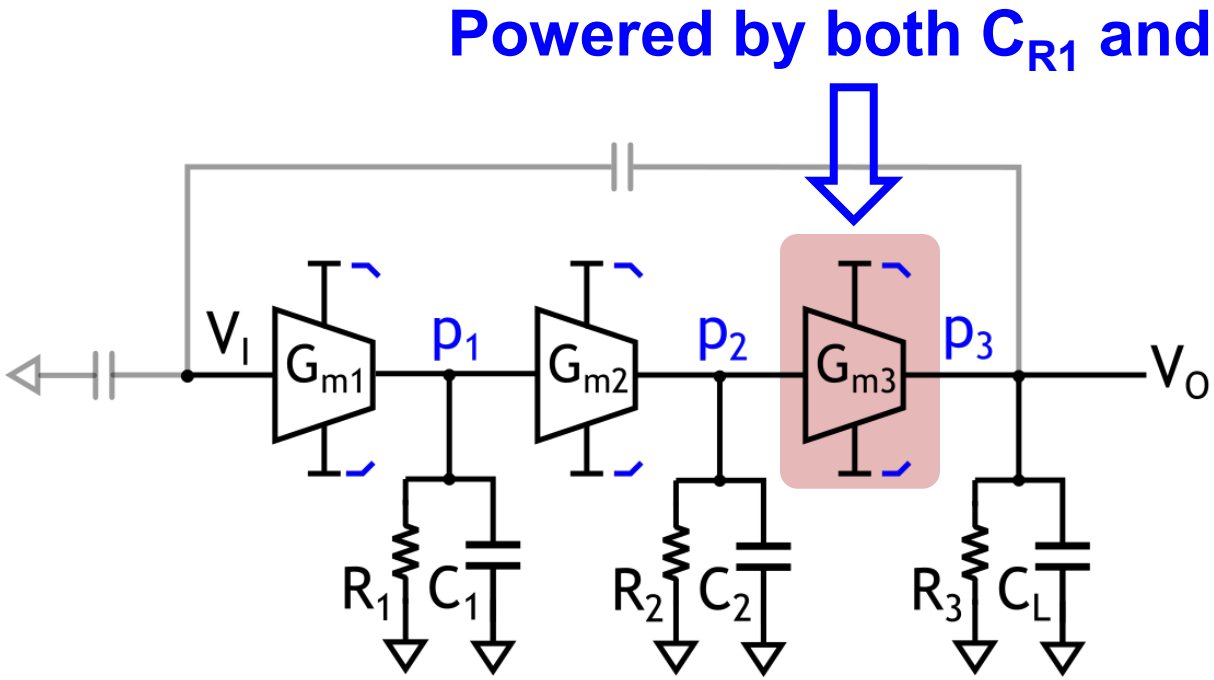
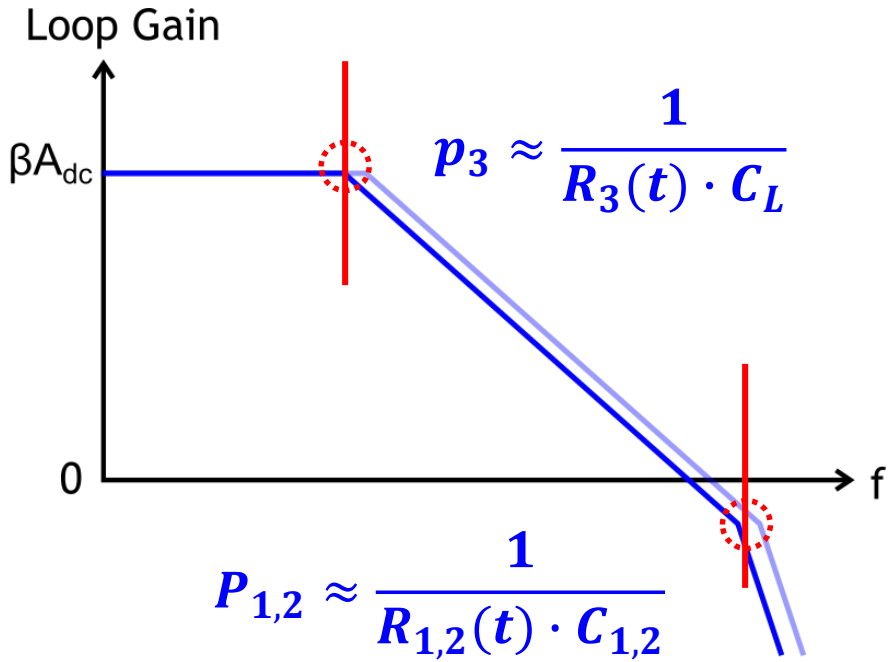




Proposed 3-stage Cascoded FIA

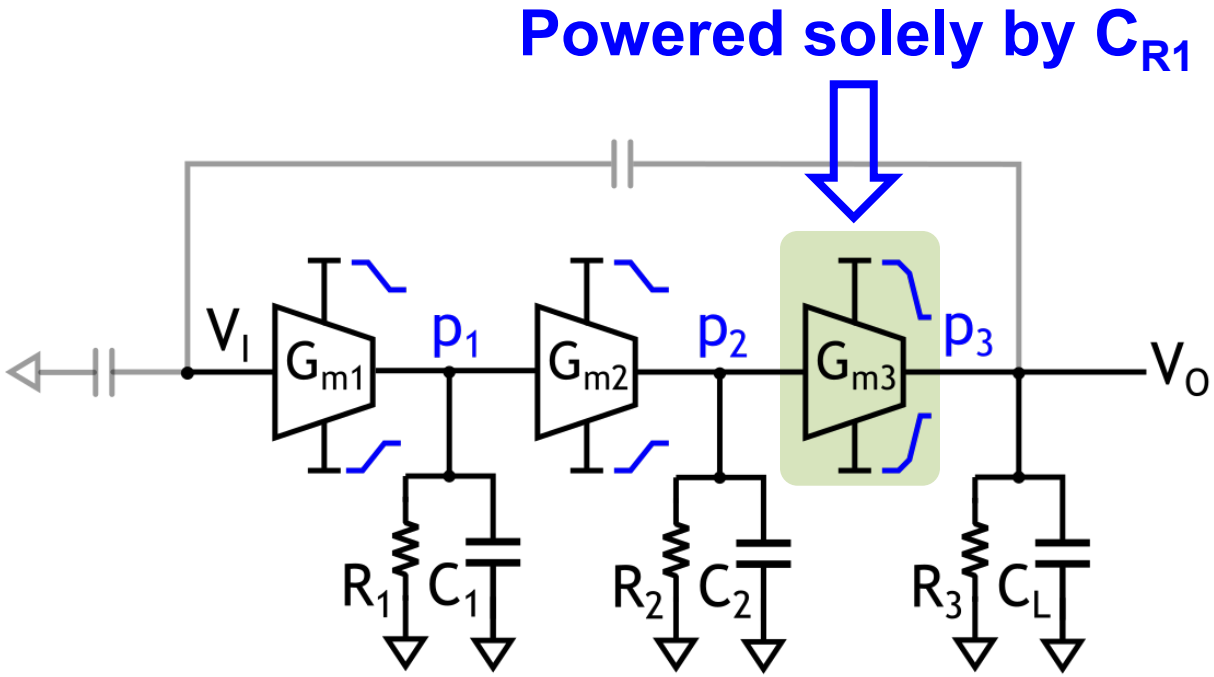
- Closed-loop 3-stage FIA design
  - –Fast settling step

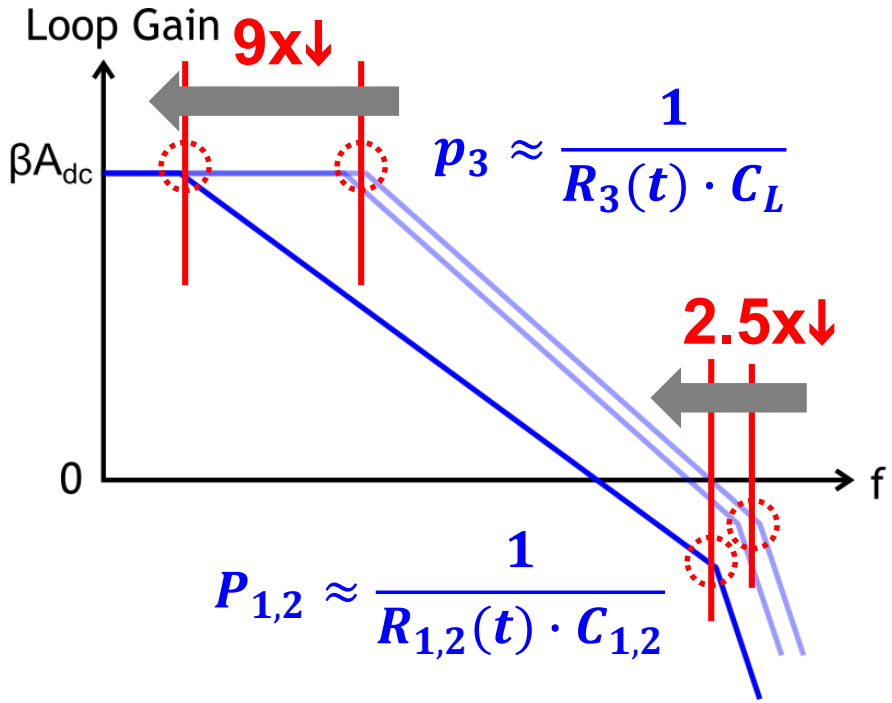




Proposed 3-stage Cascoded FIA

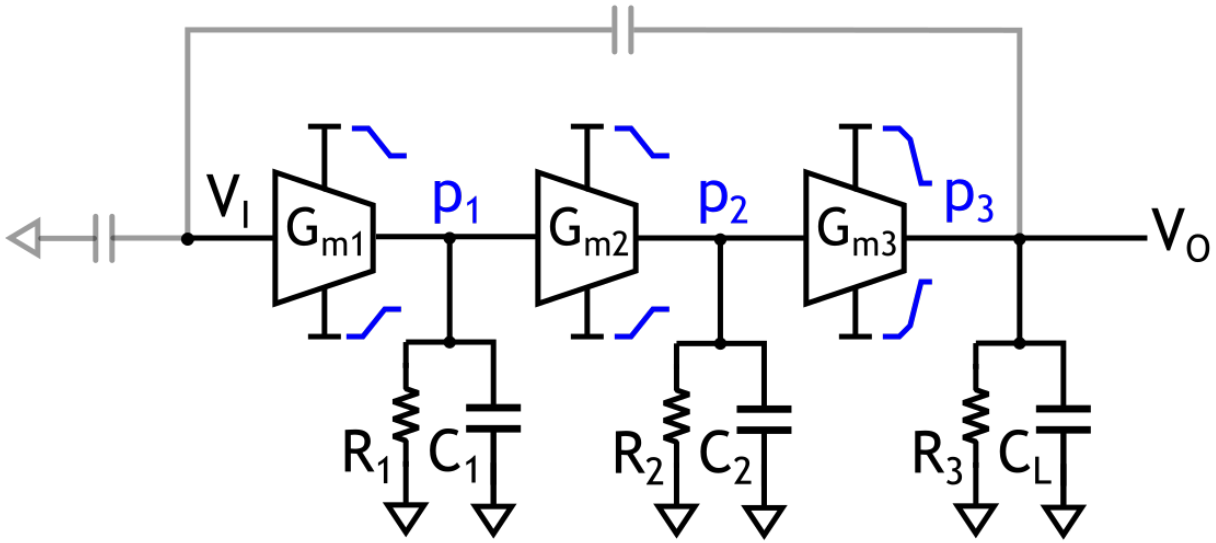
- Closed-loop 3-stage FIA design
  - –Dominate pole shifts inward faster to ensure stability

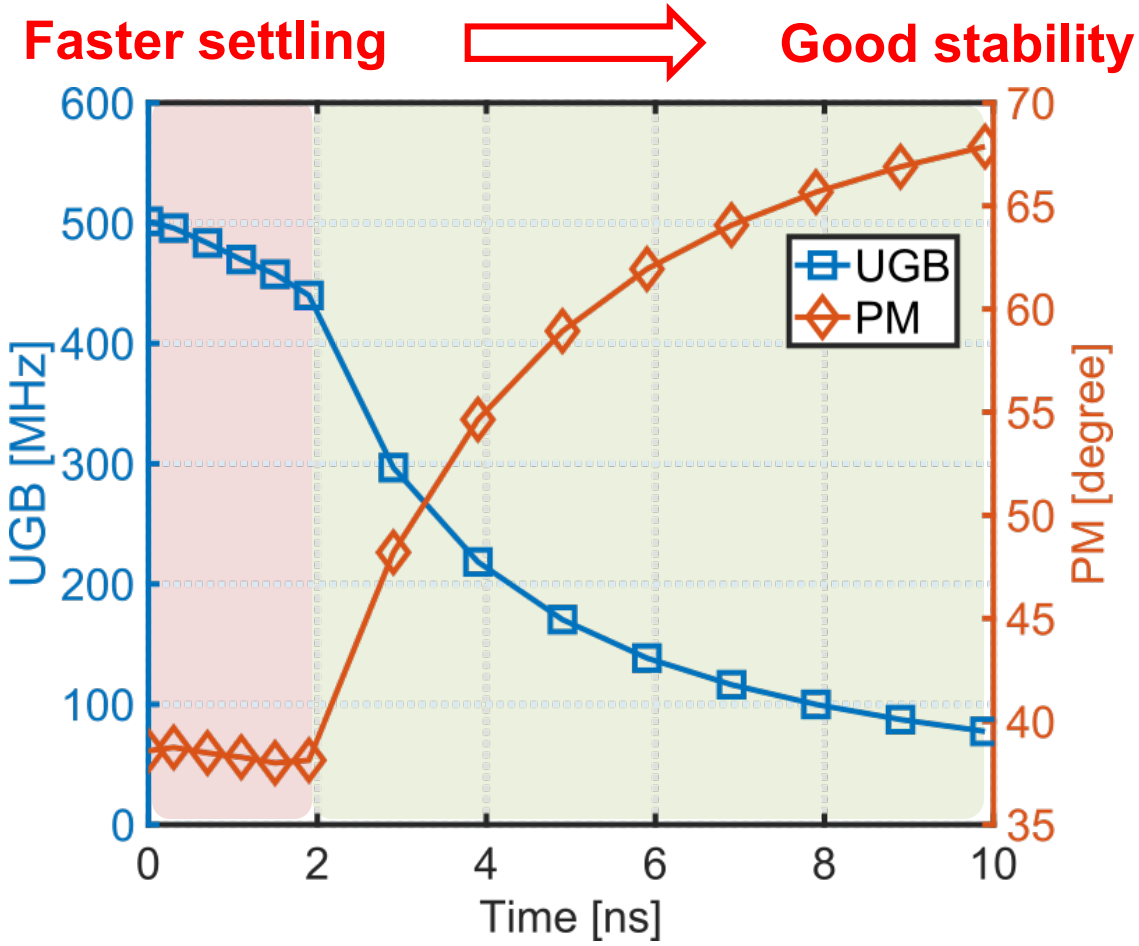




Proposed 3-stage Cascoded FIA

- Closed-loop 3-stage FIA design
  - –Dynamically scaled BW ☺

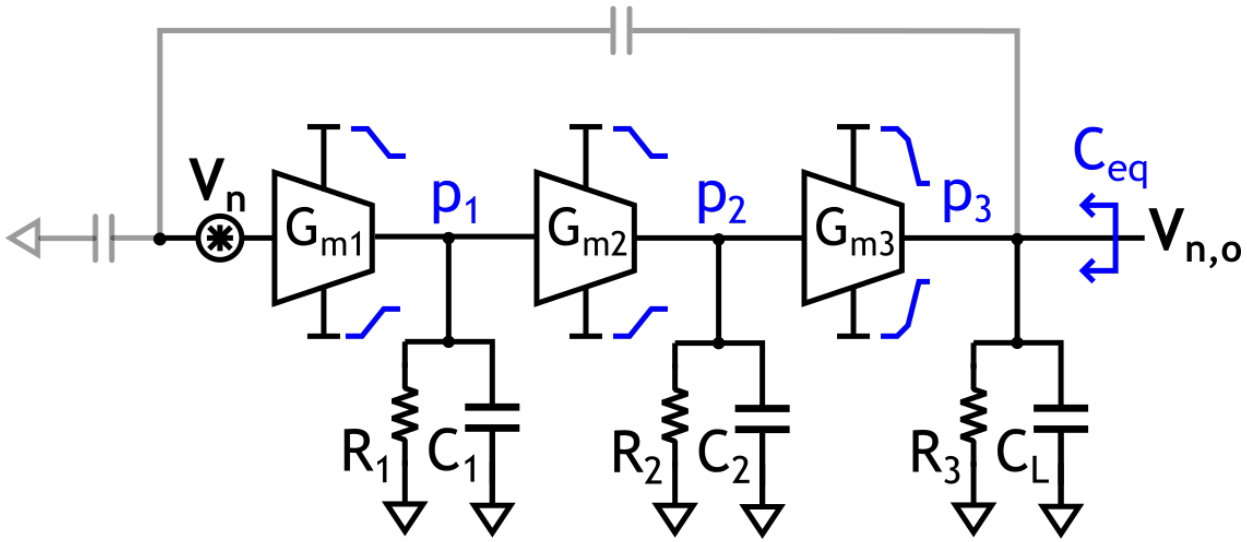


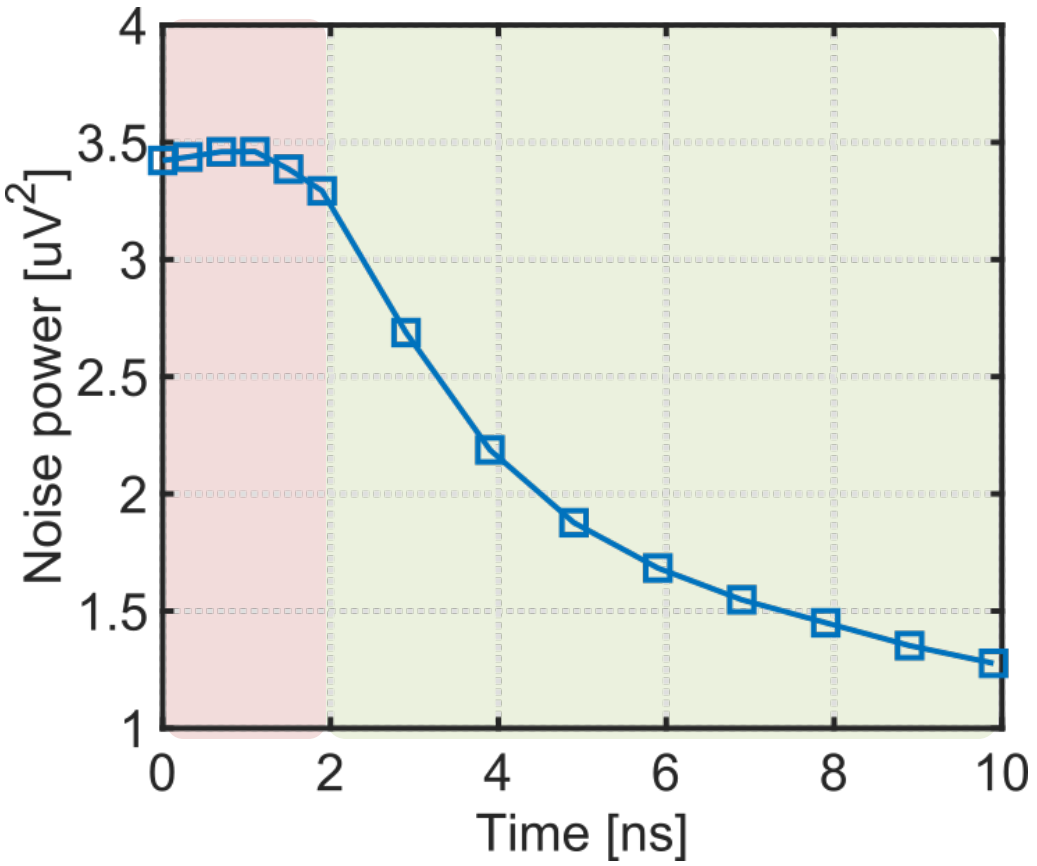


Proposed 3-stage Cascoded FIA

- Closed-loop 3-stage FIA design
  - –Reduced noise ☺
  - –$G_{m3}R_1$ drops with time

$$\overline{v_{n,o}^2} \approx \frac{kT}{\beta C_{eq}} \cdot (G_{m2}R_2) \cdot (G_{m3}R_1)$$





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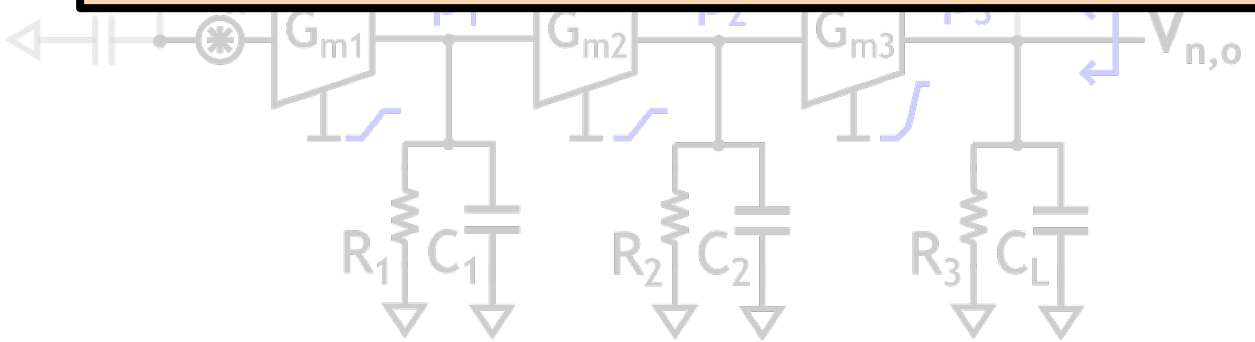
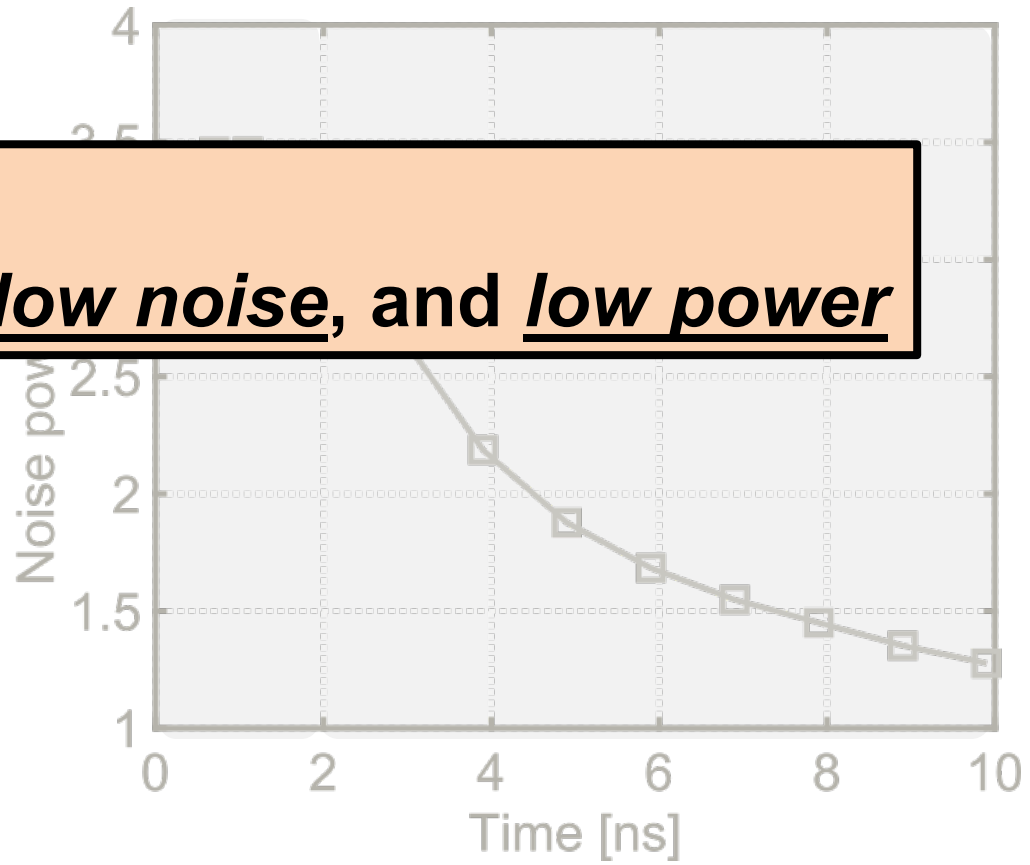
  - –Reduced noise ☺
  - –$G_{m3}R_1$ drops with time

$$\overline{v_{n,o}^2} \approx \frac{kT}{\beta C_{eq}} \cdot (G_{m2}R_2) \cdot (G_{m3}R_1)$$

Initial high BW for *fast settling*
Decaying BW for *good stability*, *low noise*, and *low power*





Proposed 3-stage Cascoded FIA

- Closed-loop 3-stage FIA design
  - 3-stage operation + self-biased dynamic cascode
    - 82dB DC gain
  - Two-step operation + dynamically scaled BW
    - Settling, stability, and noise

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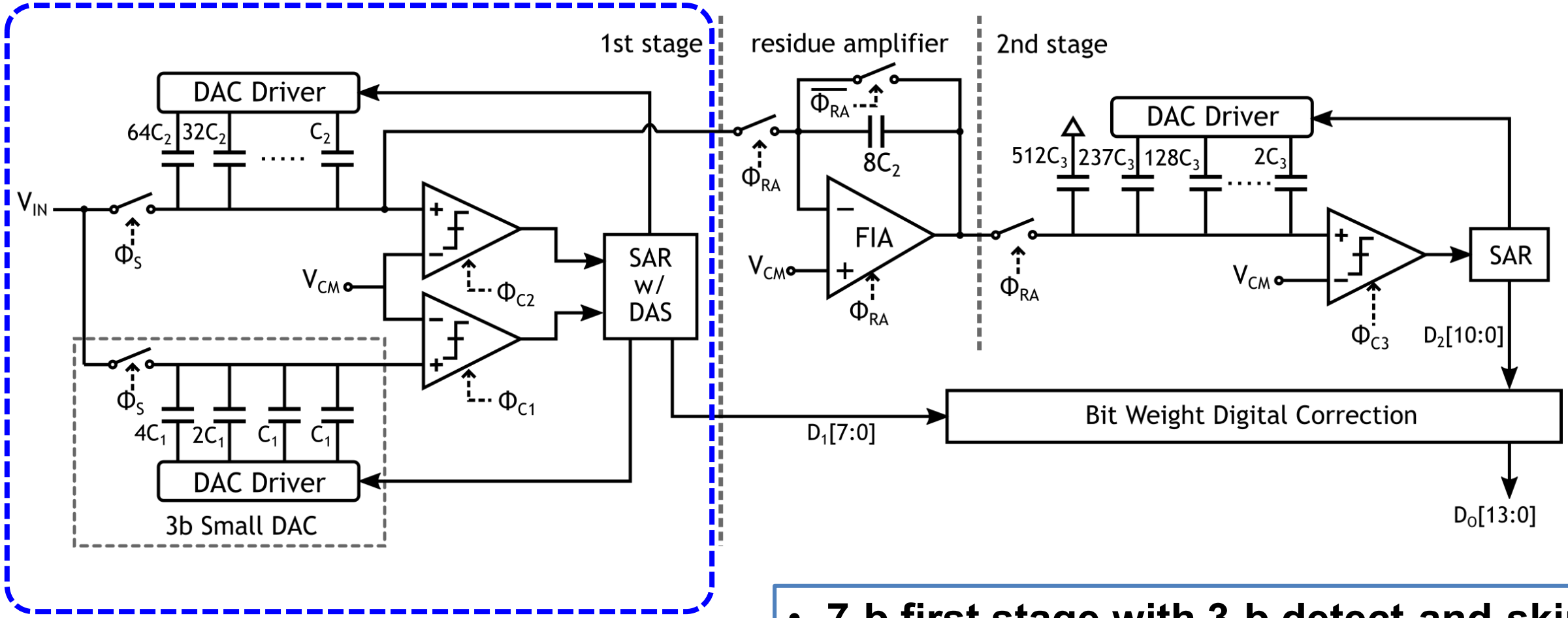
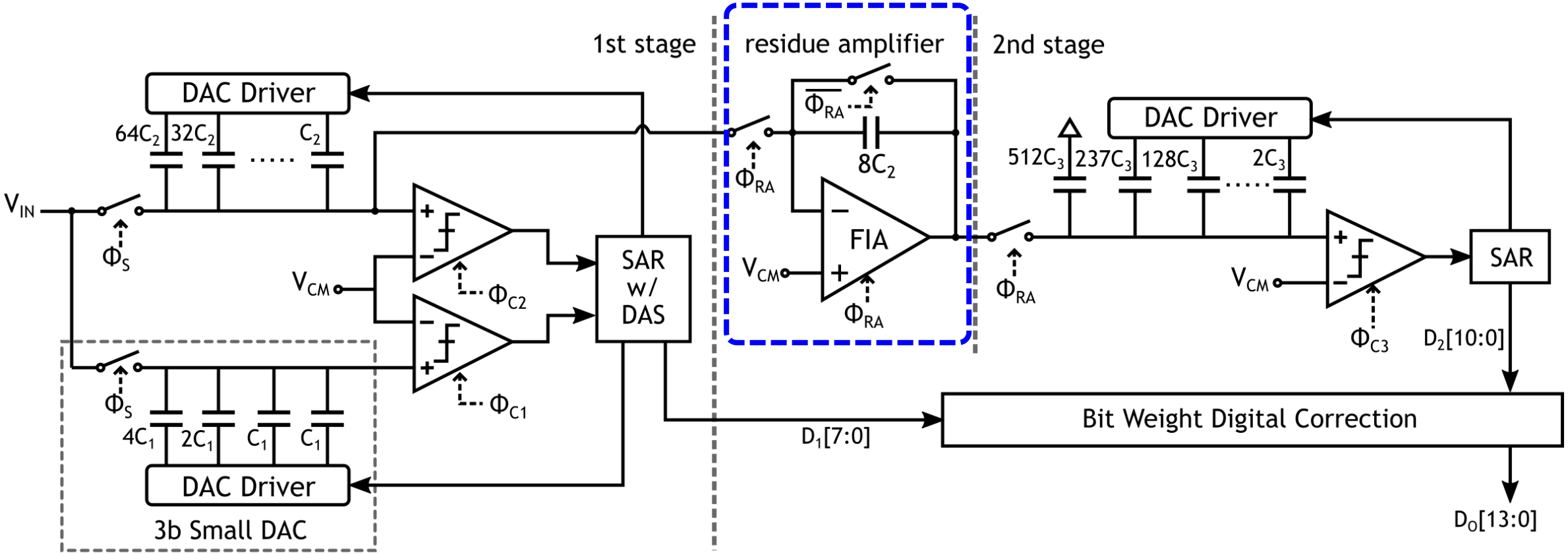
Pipelined SAR Design



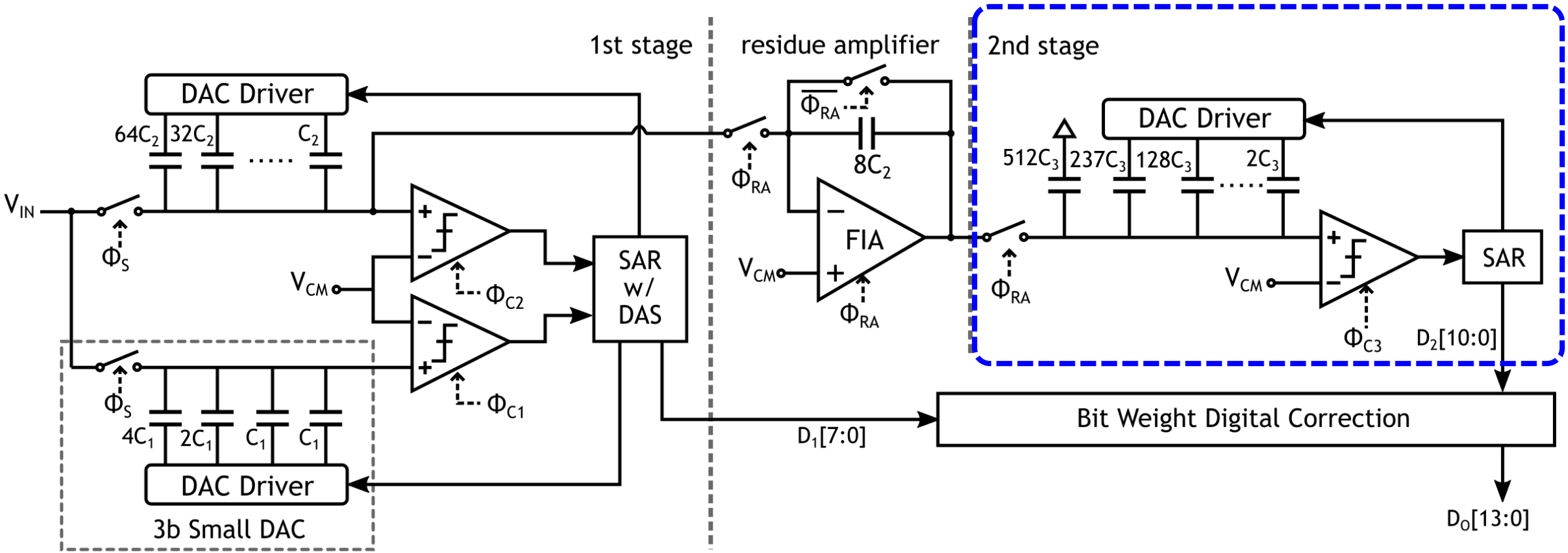
- 7-b first stage with 3-b detect-and-skip
  - $C_{DAC,L}$ = 4pF; $C_{DAC,S}$ = 80fF

Pipelined SAR Design



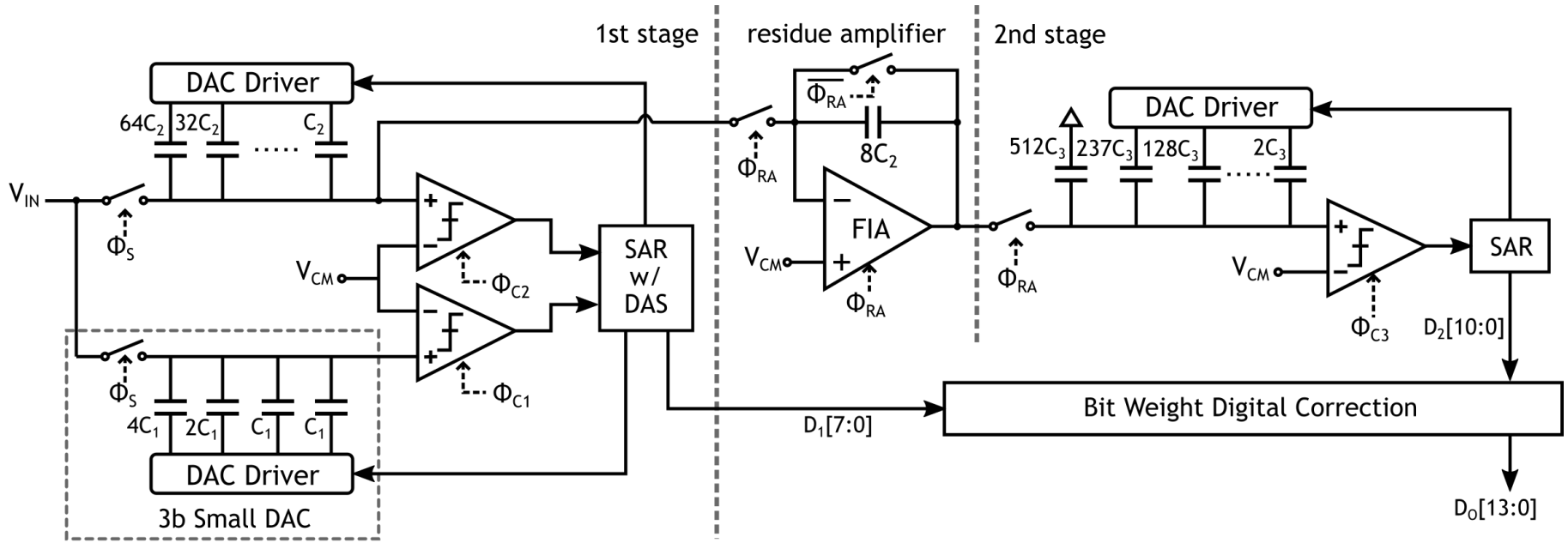
- 32x dynamic residue amplification
  - 16x closed-loop FIA gain
  - 2x reference scaling

Pipelined SAR Design



- **9-b second stage SAR**
  - **C_{DAC} = 0.5pF**

Event-Driven Operation



Event

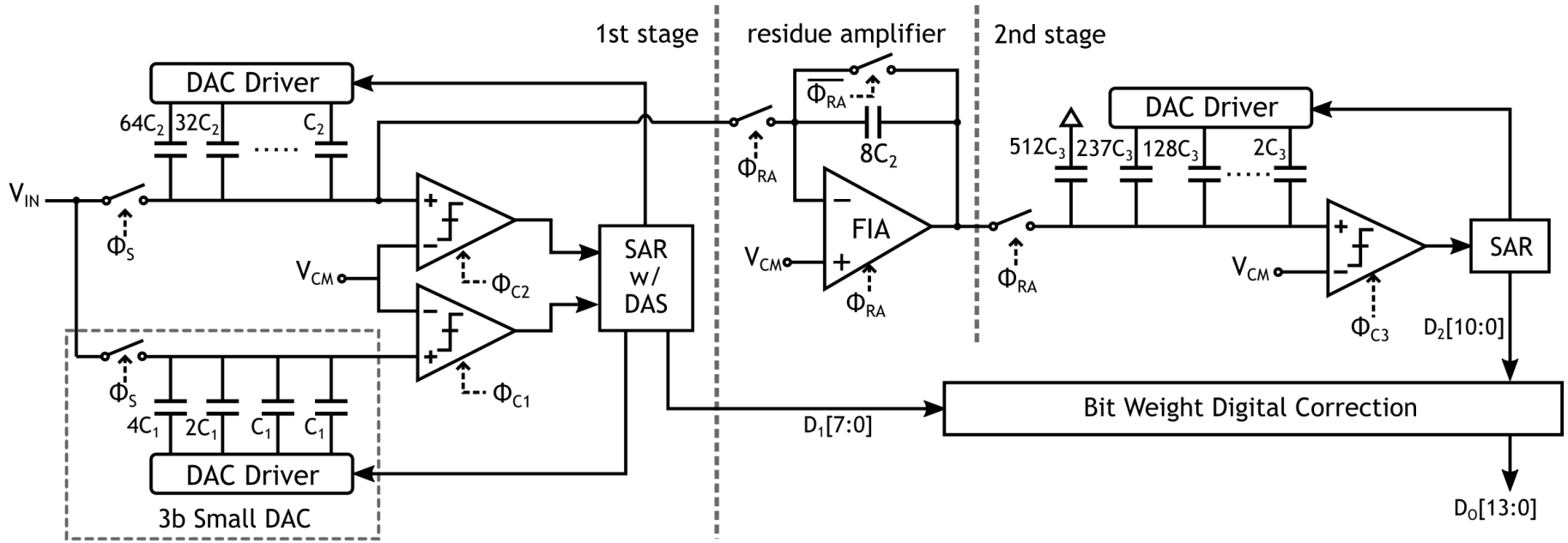
1st stage track

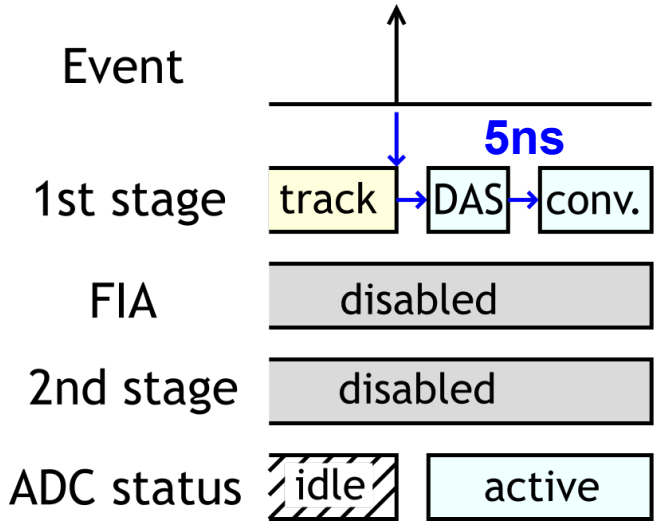
FIA disabled

2nd stage disabled

ADC status idle

Event-Driven Operation





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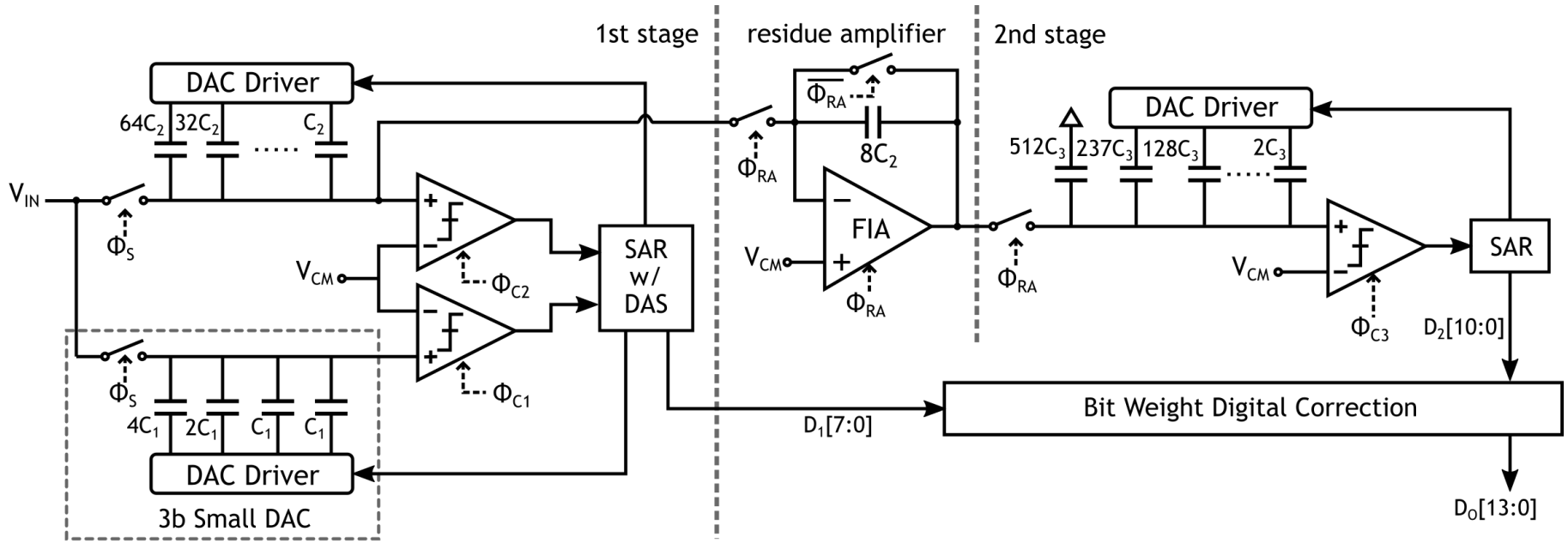
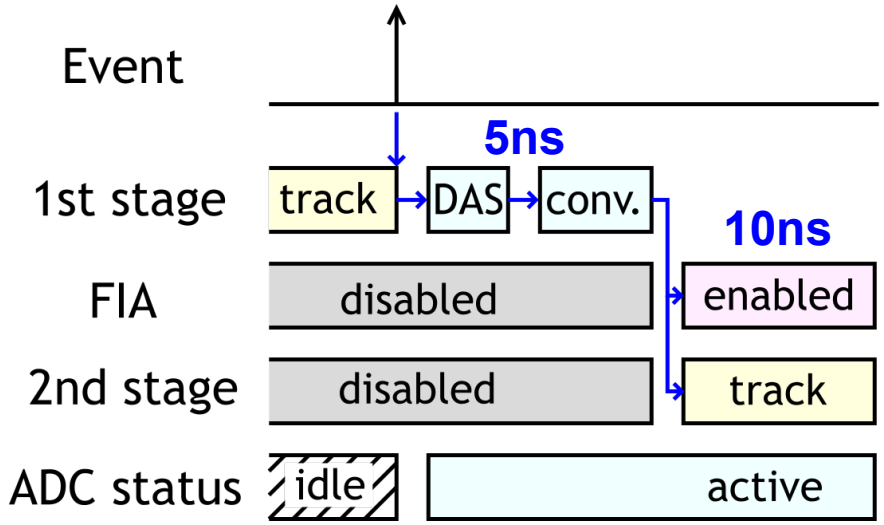
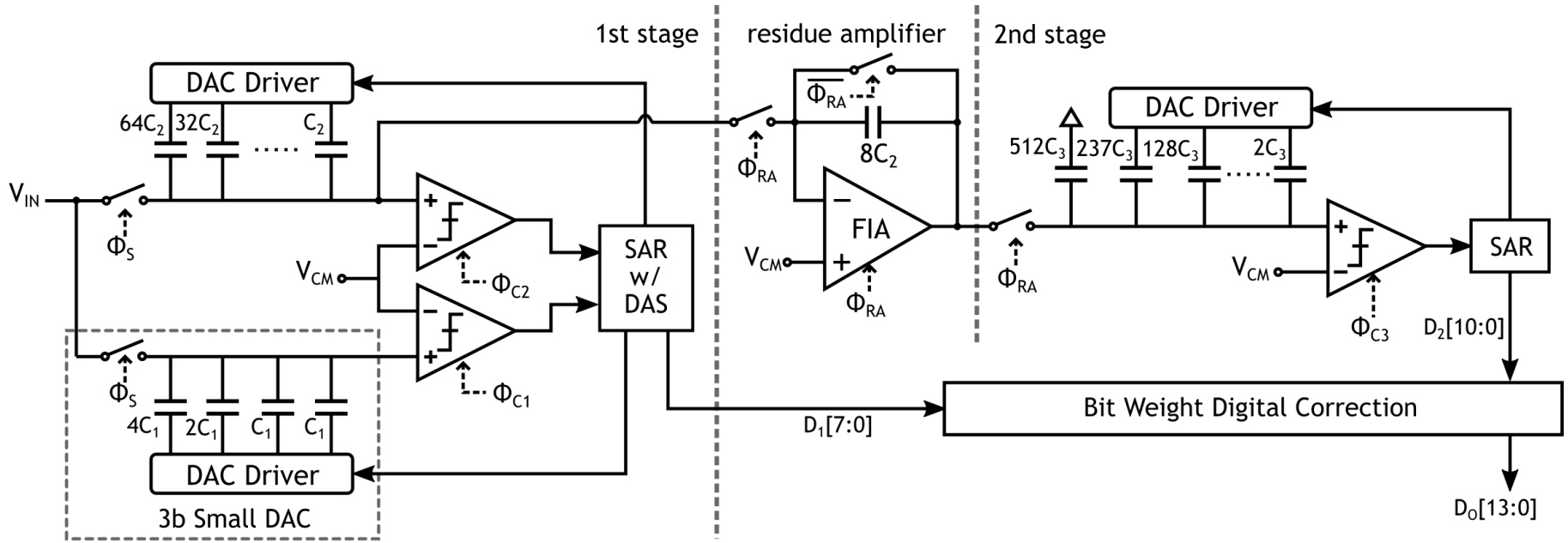
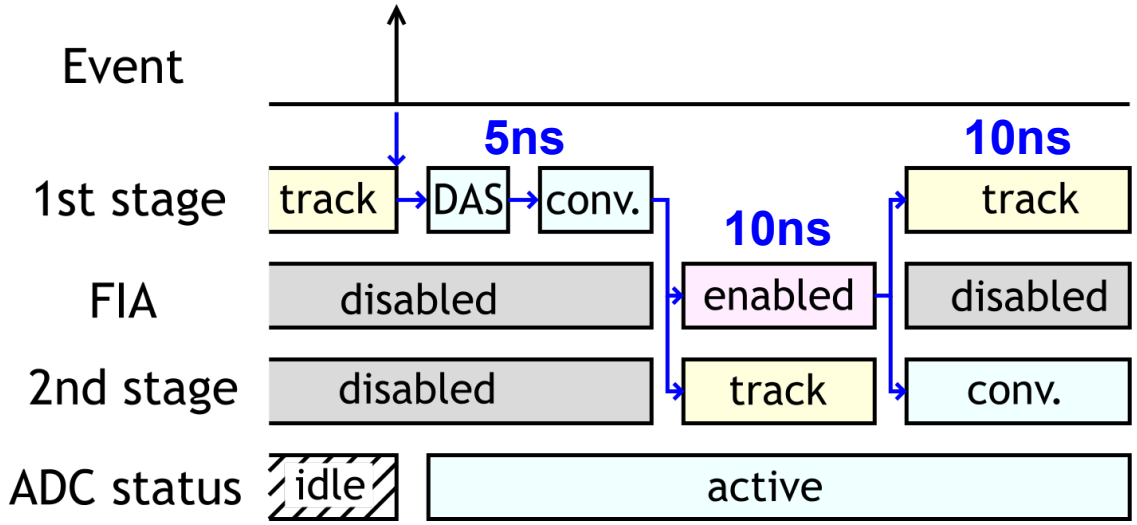


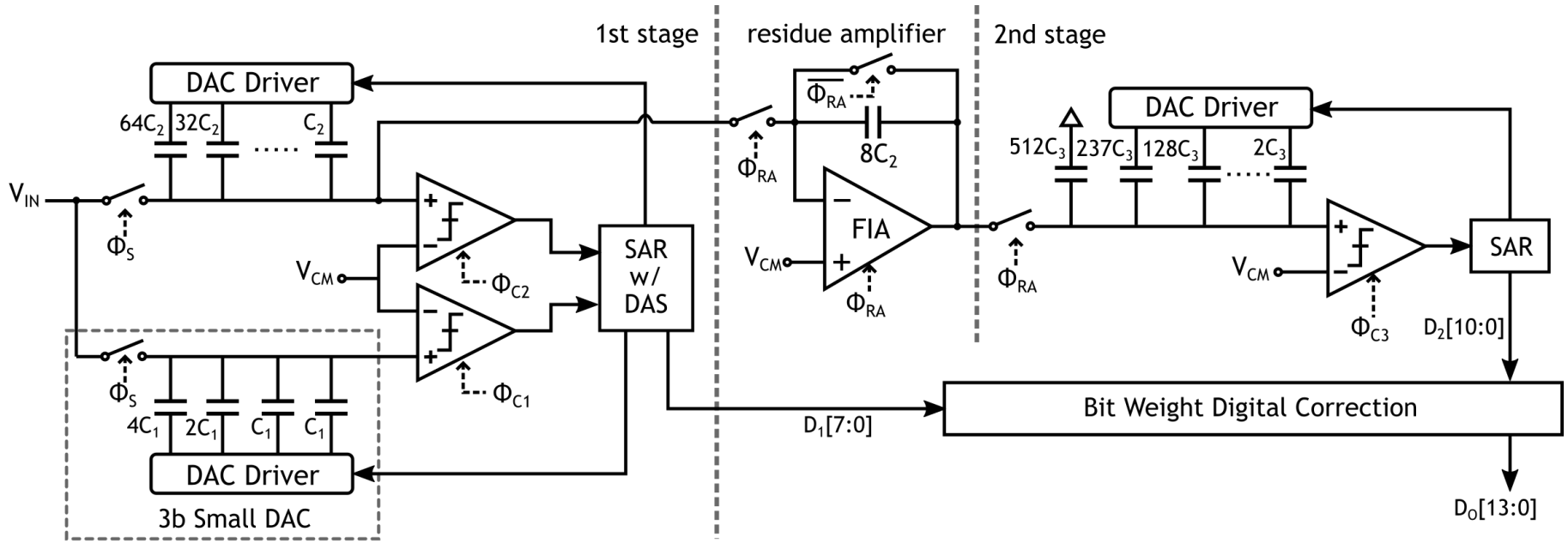


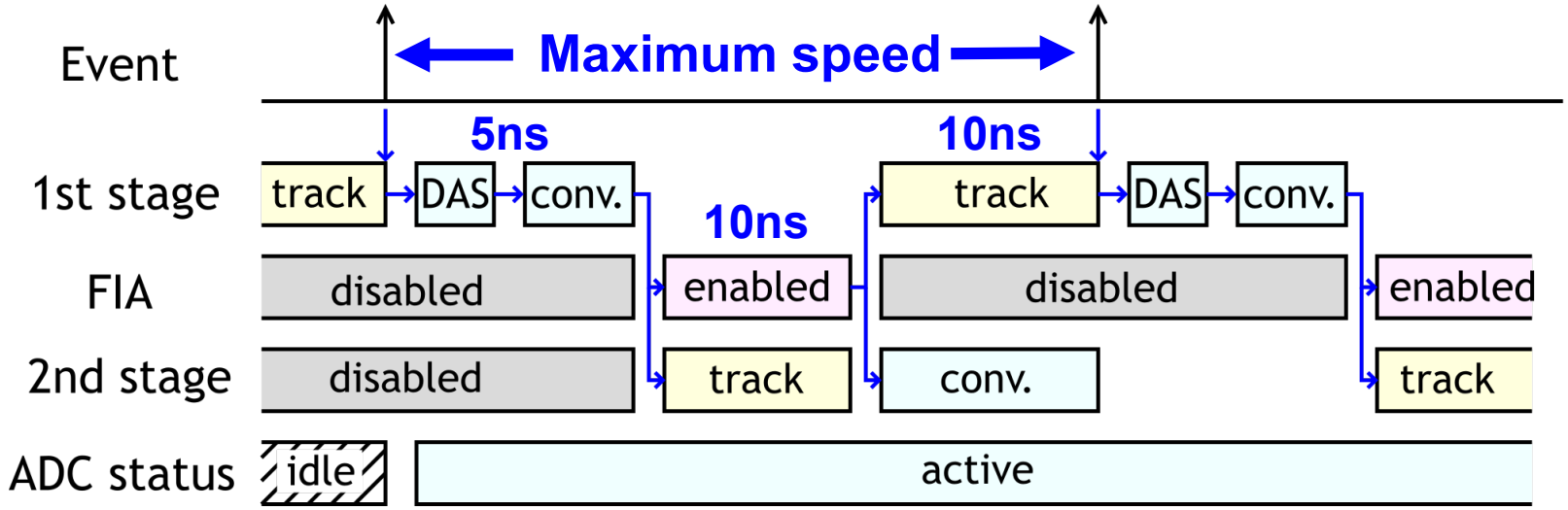
Event-Driven Operation



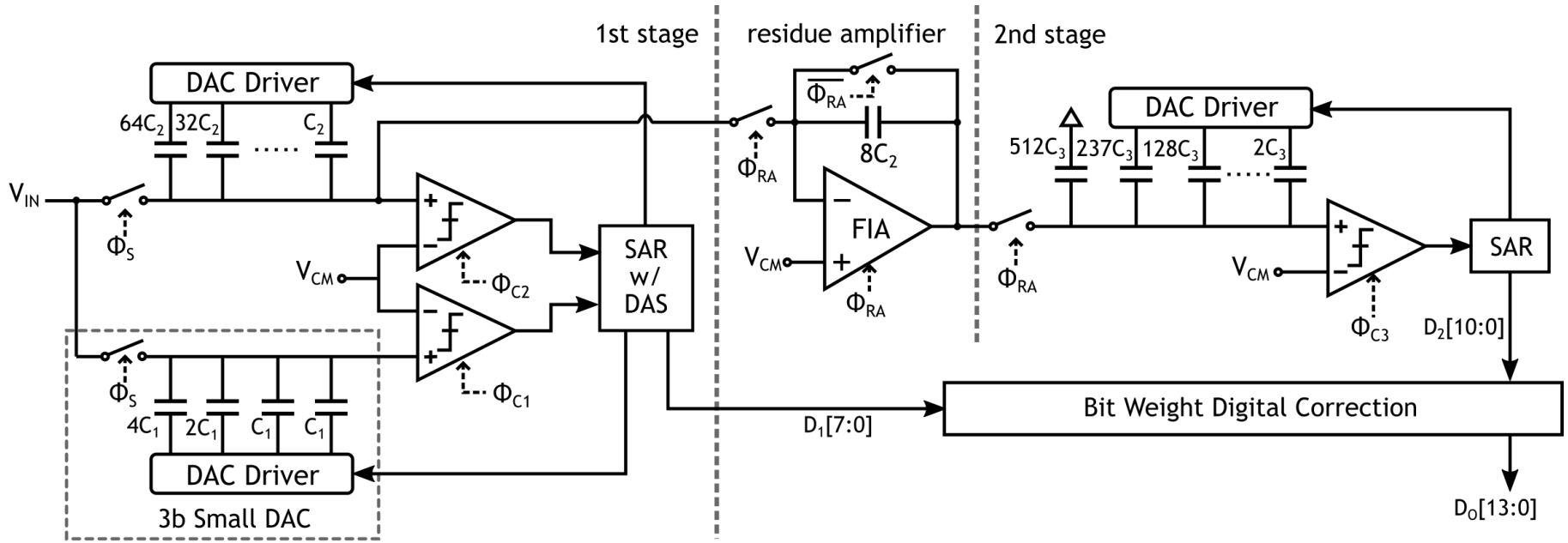


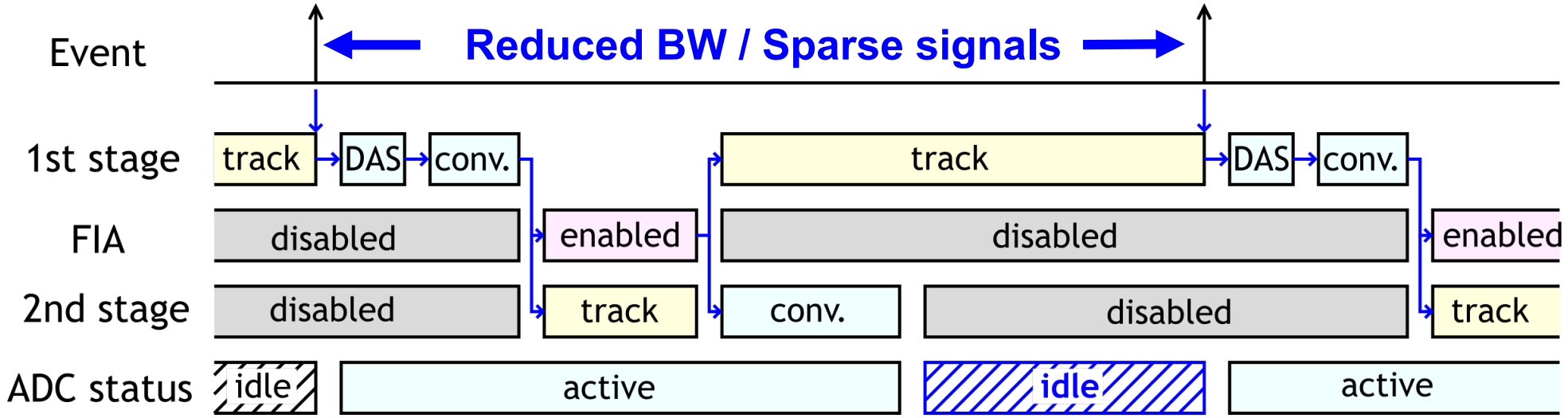
Event-Driven Operation



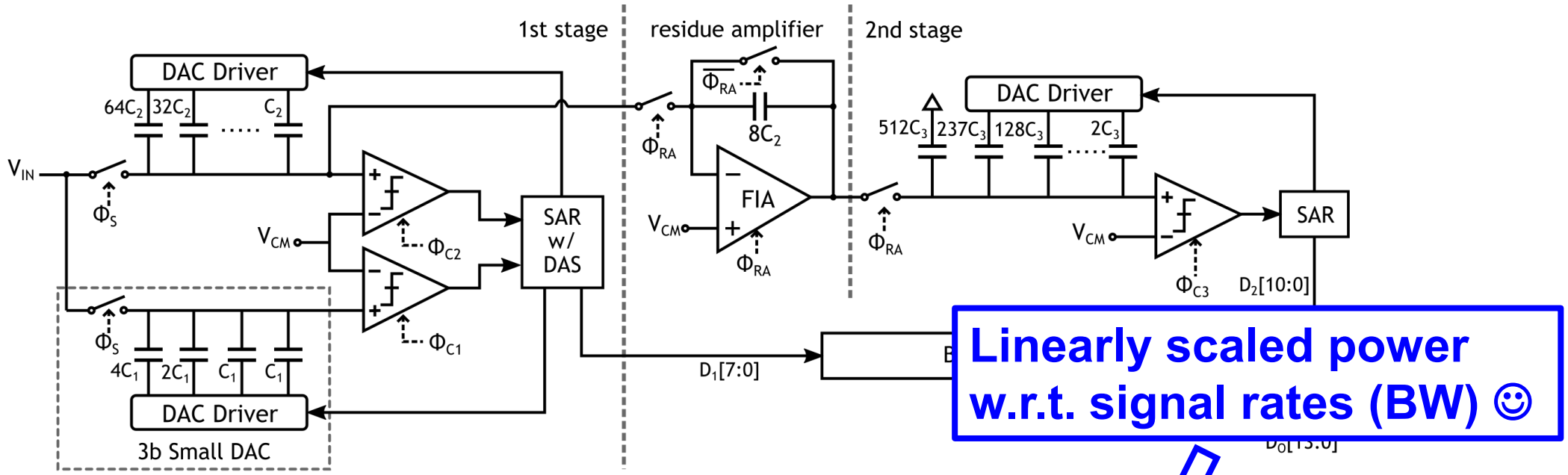


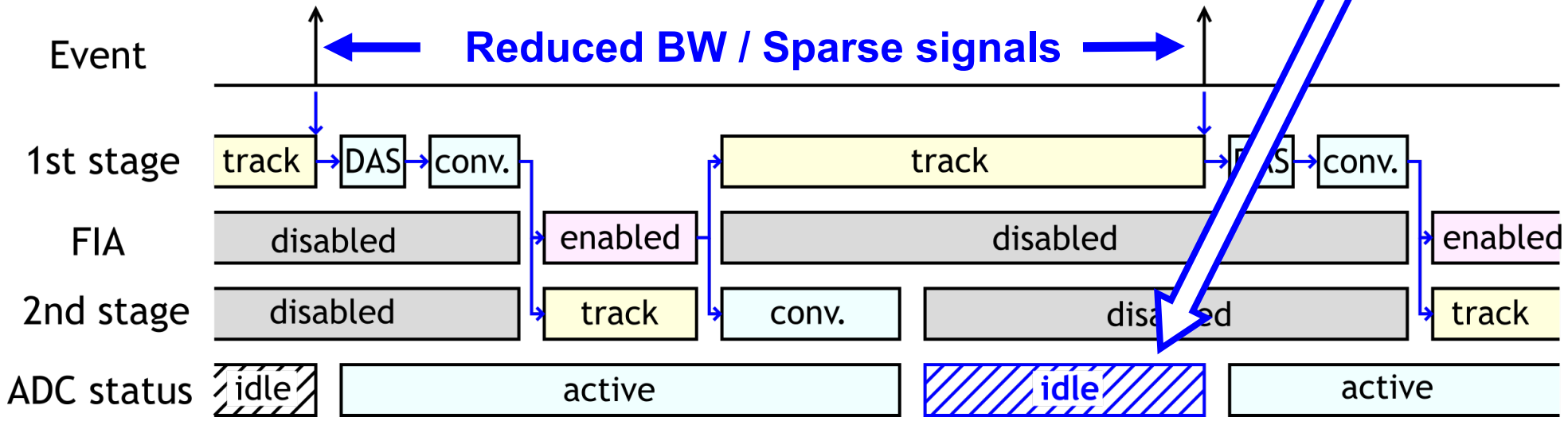
Event-Driven Operation





Event-Driven Operation



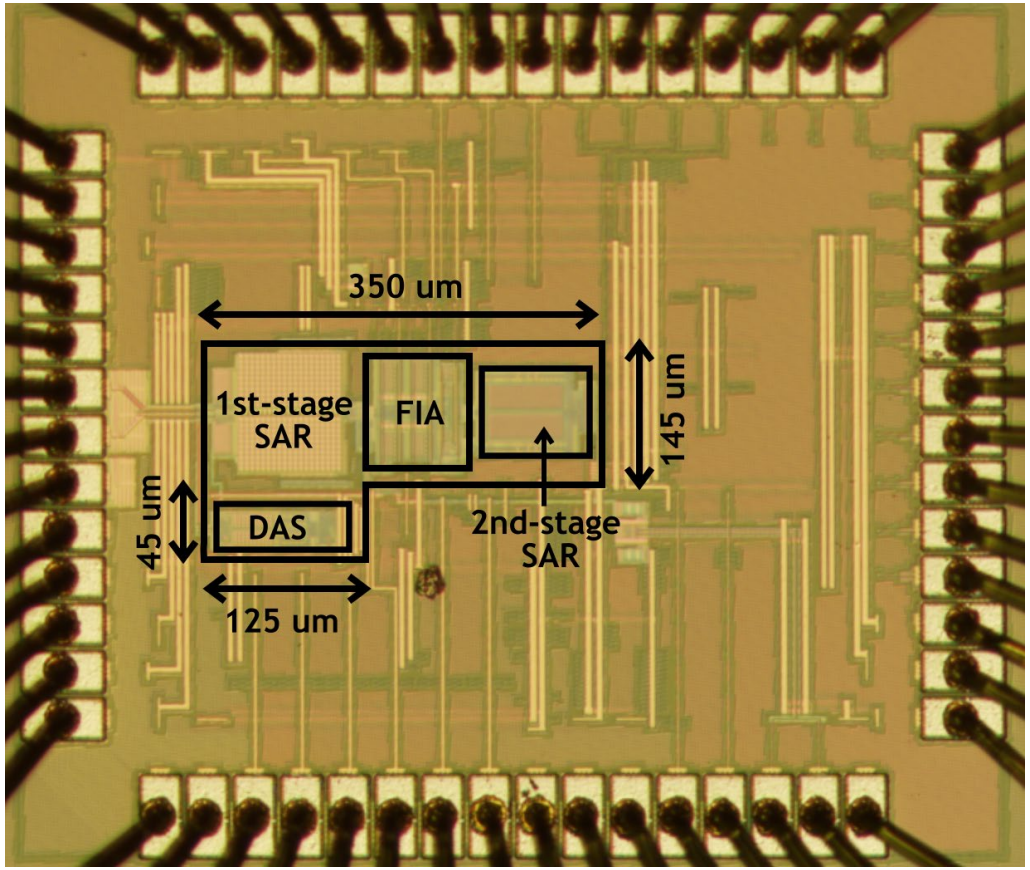


Outline

- Motivation
- Proposed Cascoded Floating Inverter Amplifier (FIA)
- Pipelined SAR Circuit Implementation
- **Measurement Results**
- Conclusion

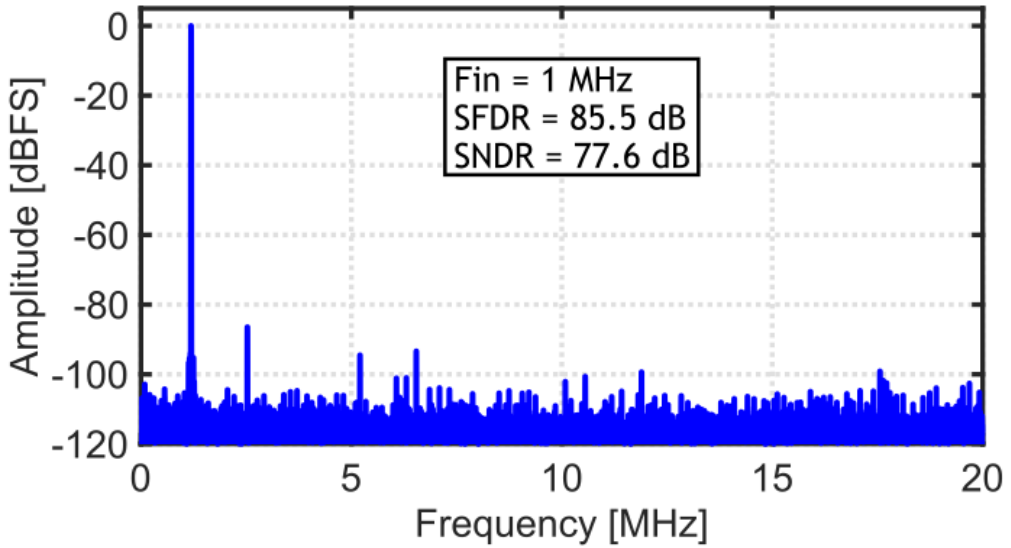
Chip Micrograph

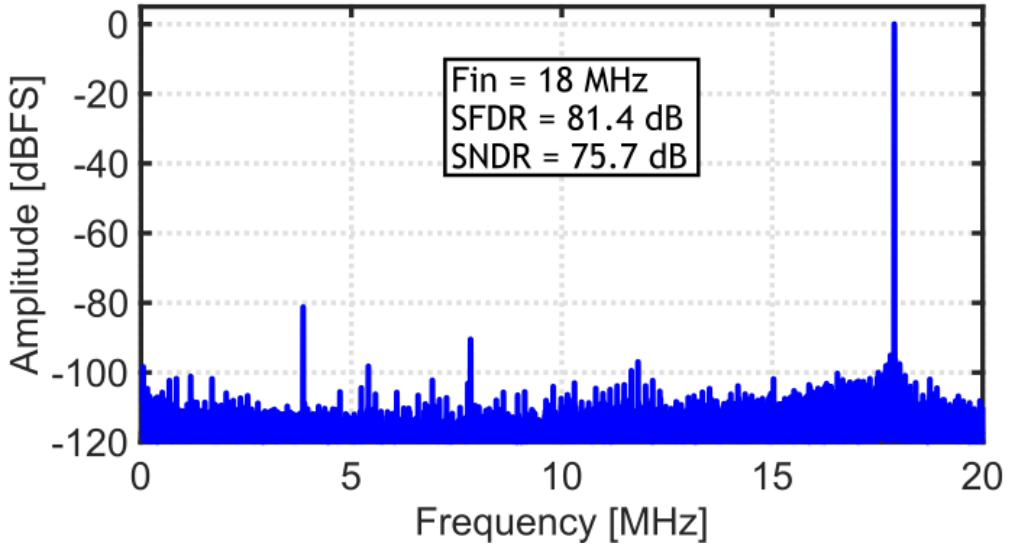
- 40nm LP CMOS
- Active Area: 0.056mm^2
- Supply: 1.2V
- Fs: 0.4-40MHz
- Highest BW: 20MHz



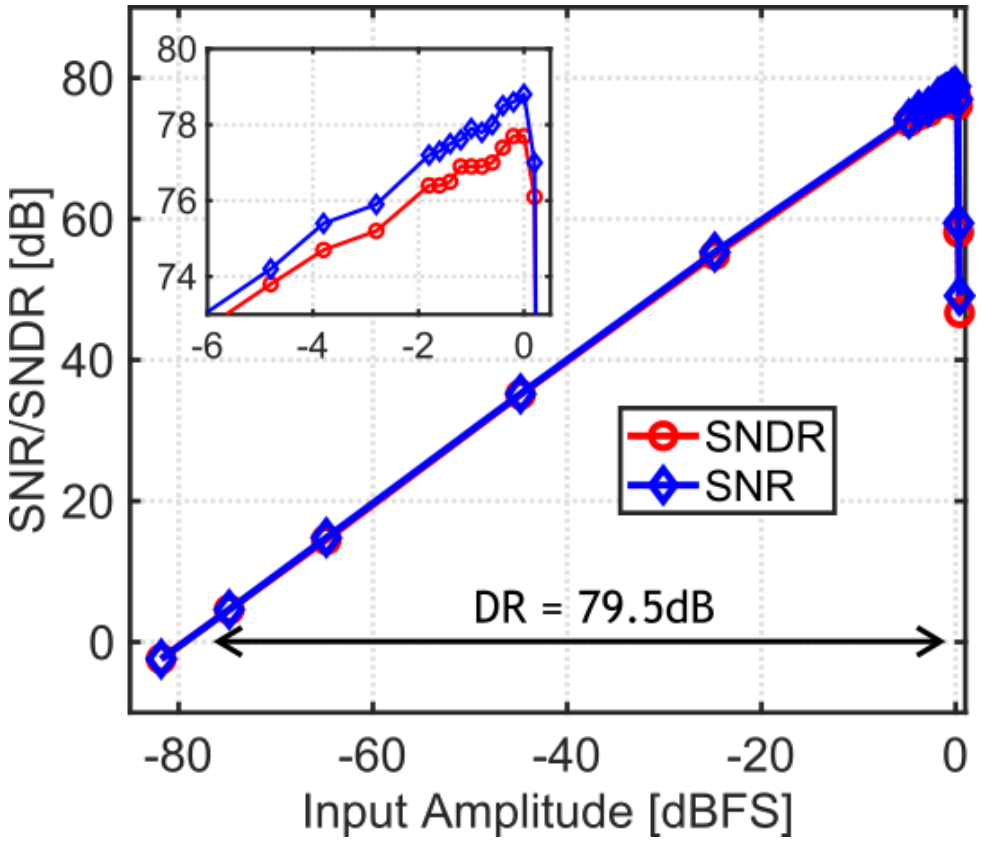
Measured Spectra @ 40MHz

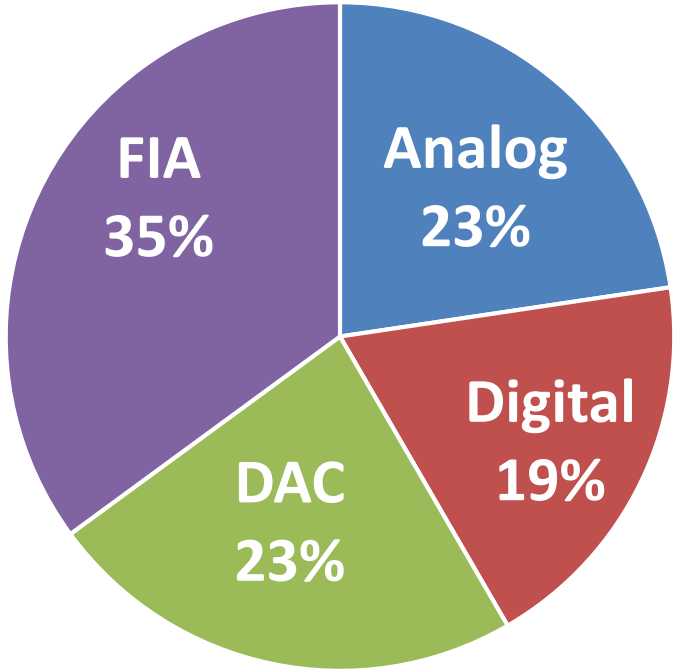
- LF input @ 1MHz
  - SFDR: 85.5dB
  - SNDR: 77.6dB
- HF input @ 18MHz
  - SFDR: 81.4dB
  - SNDR: 75.7dB





DR & Power Breakdown

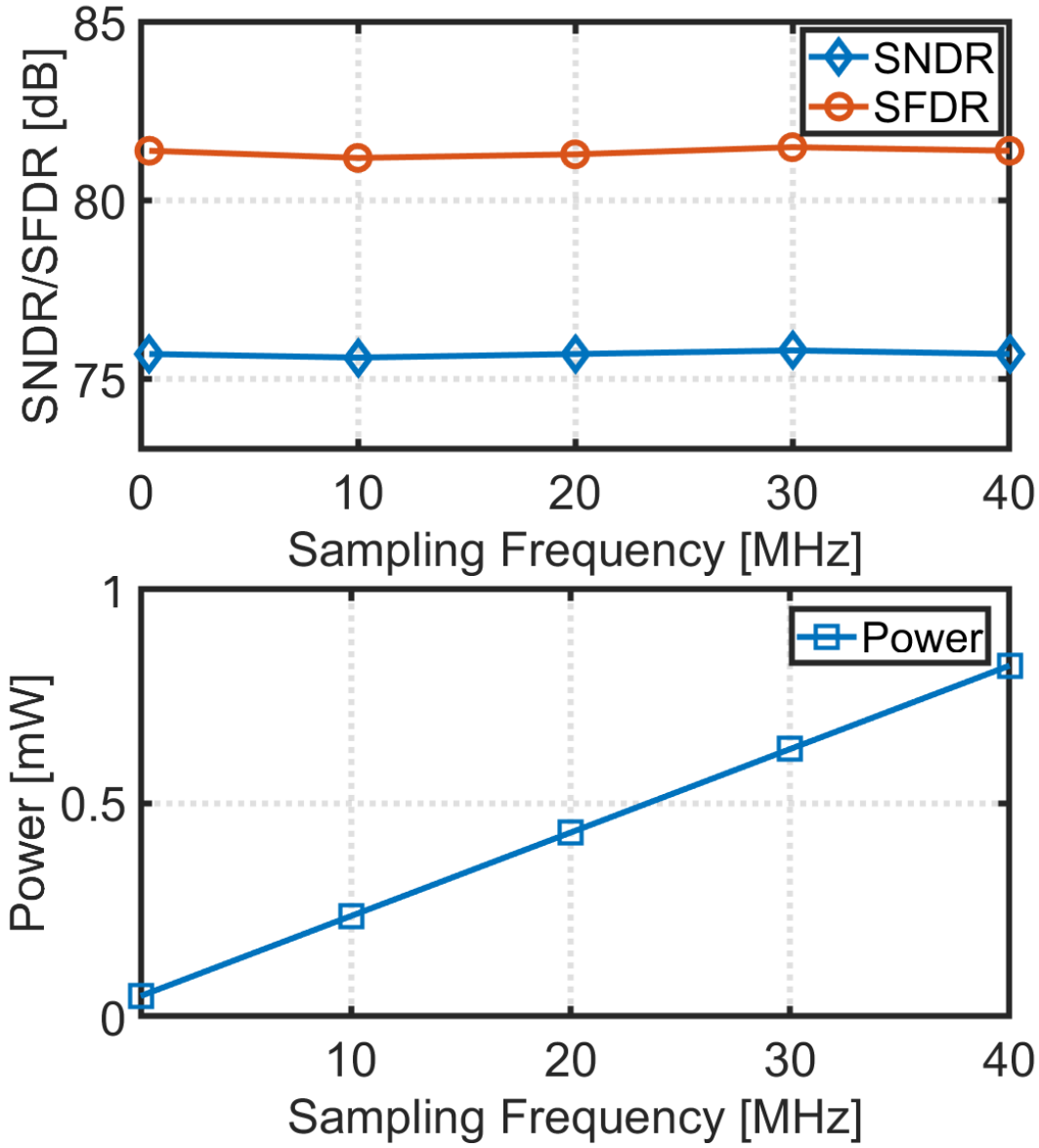




- **Measured DR: 79.5 dB**
- **Power: 821uW @ 40MS/s**

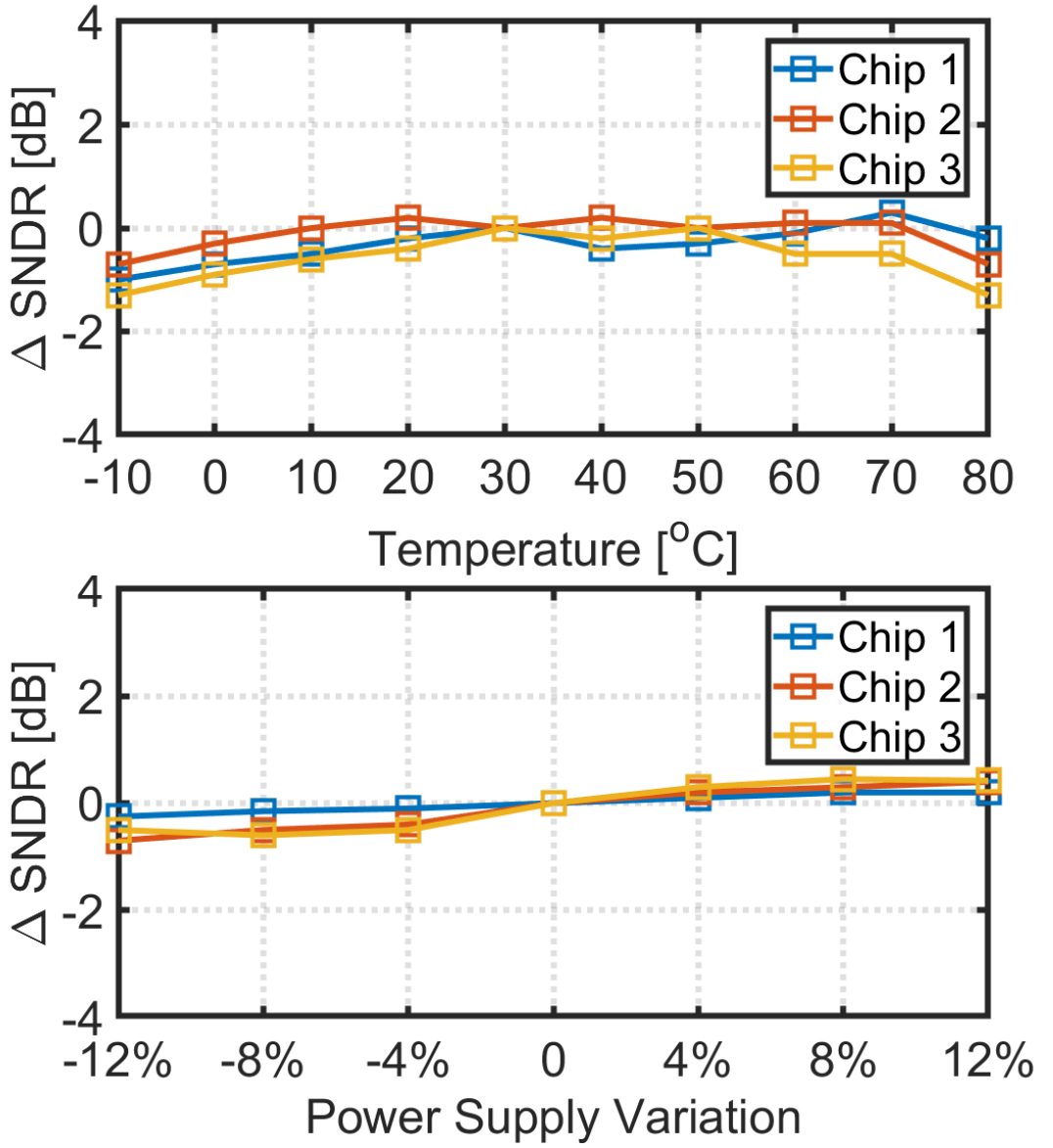
Measured Fs Variations

- **Sampling frequency**
  - **–0.4MHz to 40MHz**
- **Negligible performance variation**
- **Linearly scaled power**



Measured Temp/Voltage Variations

- **Temp: -10°C ~ 80°C**
  - **–Within 2 dB variation**
- **Voltage: -12% ~ 12%**
  - **–Within 1 dB variation**



Comparison with Prior Works

	ISSCC 15 Lim	ISSCC 19 ElShater	ISSCC 20 Hung	ISSCC 19 Hershberg	This work
Architecture	Pipe-SAR	Pipe-SAR	Pipe-SAR	Pipe-SAR	**Pipe-SAR**
Process [nm]	65	180	28	16	**40**
Residue Amp	Ring amp	Ring amp	Ring amp	Ring amp	**FIA**
Stabilization	Deadzone	Deadzone	Deadzone	Deadzone	**Self-quenching**
Sampling Freq. Scalability	N/A	N/A	N/A	100x	**100x**
Fs [MS/s]	50	15	100	6-600	**0.4-40**
Area [mm^2]	0.054	1.82	0.018	0.037	**0.056**
Power [mW]	1	9.82	0.7	6	**0.82**
SNDR [dB]	70.9	90.8	71.7	60.2	**75.7**
FoMw [fJ/c-s]	6.9	23.1	2.2	12	**4.1**
FoMs [dB]	174.9	179.6	180.2	167.2	**179.6**

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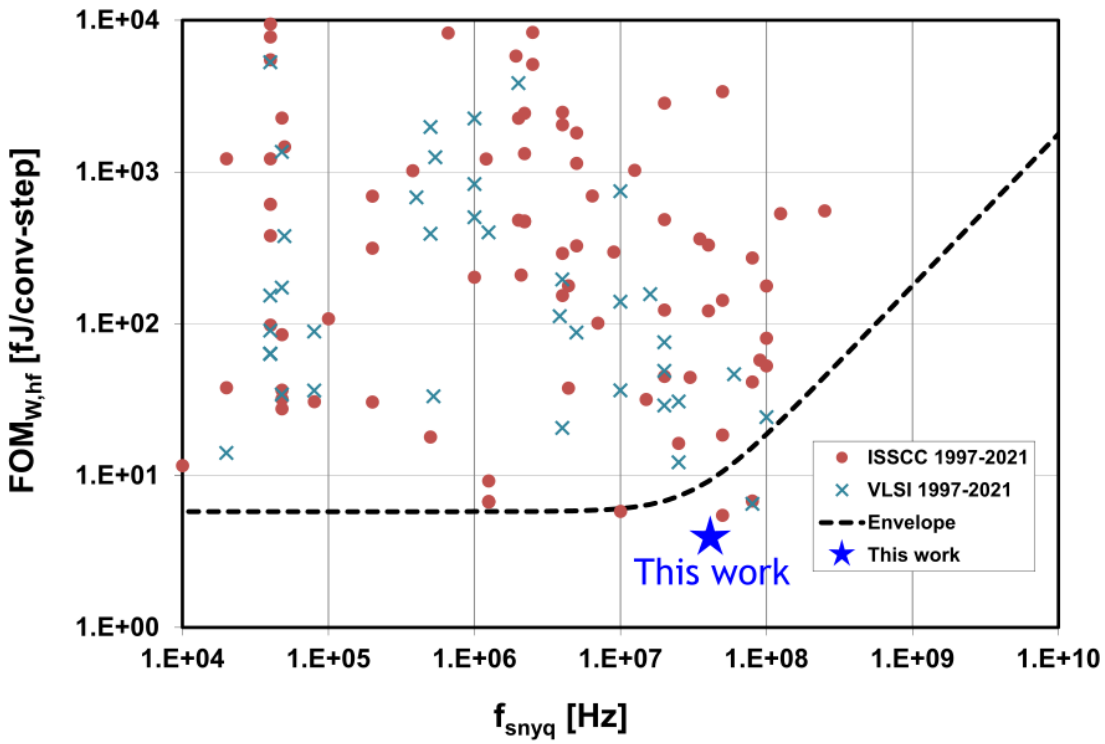
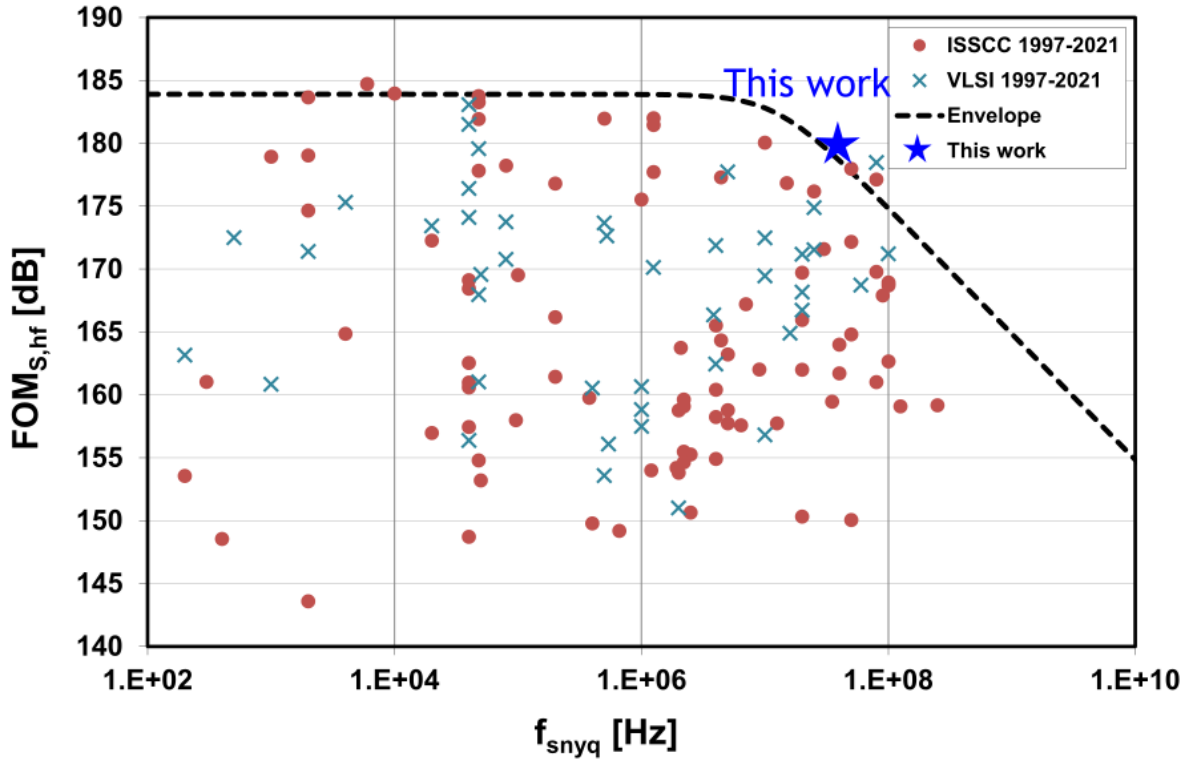
ADC Surveys (ENOB≥12)





- **Walden FoM: 4.1fJ/conv-step**
- **Schreier FoM: 179.6dB**

Conclusion

- A 3-stage cascode FIA is proposed:
  - Fully dynamic → duty-cycled operation
  - High gain → high precision
  - Dynamically scaled BW → benefits settling, stability, and noise
- Compared to the prior pipelined SAR:
  - Consistent performance and linearly scalable power over 100× sampling rate adjustment
  - Advancing state-of-the-art energy efficiency

Greetings from PRIME

- **Welcome to join us!**
  - **–Post-doc, RA openings**
  - **–xitang@pku.edu.cn**

SCAN ME

Thank you for your attention!