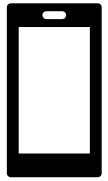
Practical Concerns and Solutions in Integrated High-Resolution ADCs

揭路

清华大学

High Resolution ADC Needs

- **General specifications**
  - **High SNDR:** >90dB
  - **High efficiency:** >175dB FoMs
  - **Med-low speed:** kHz ~ MHz BW



IoT Devices

Sensor Readout

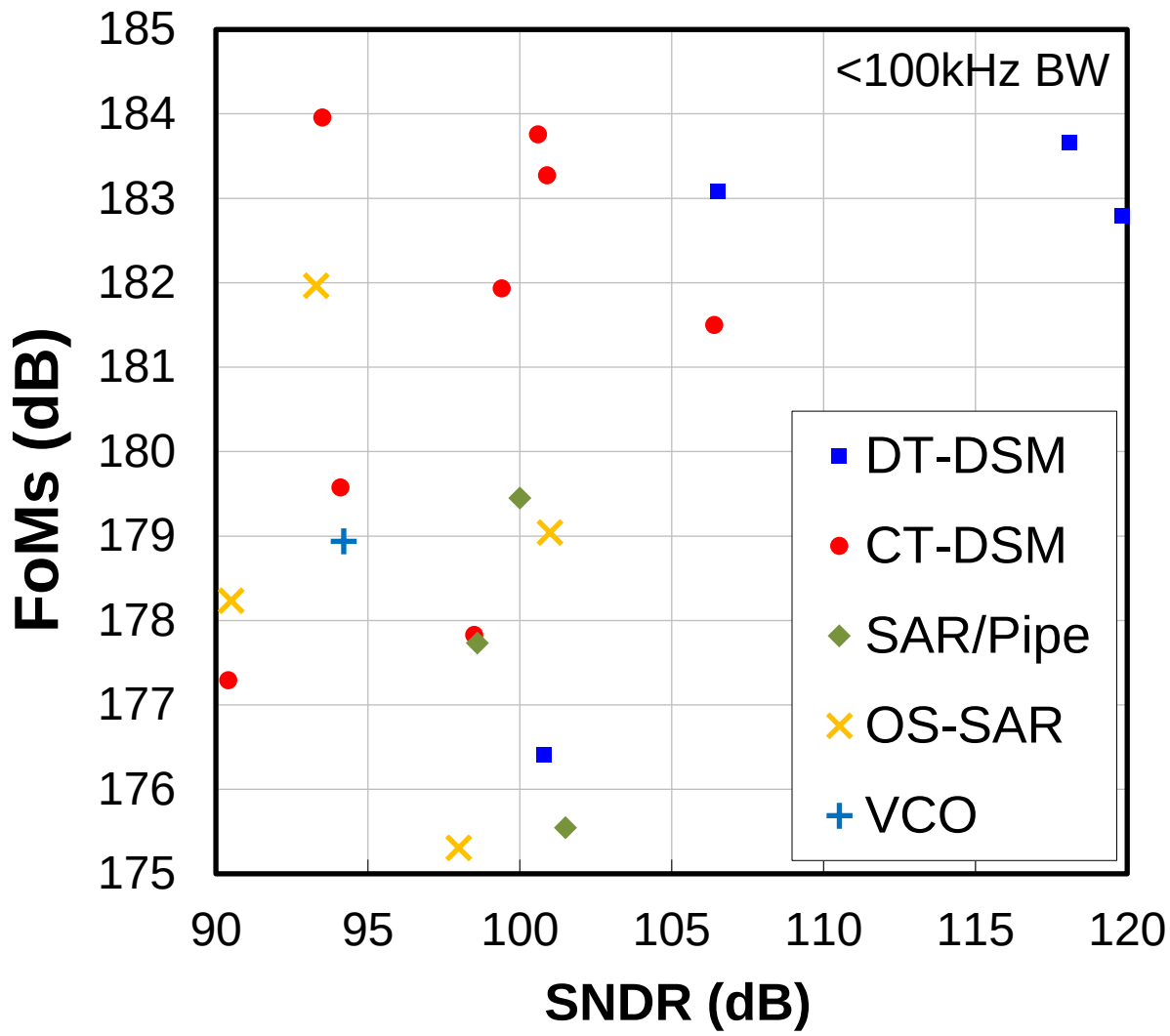
Biomedical

Acoustic

Varieties of Solutions Exist

- **General specifications**
  - **High SNDR:** >90dB
  - **High efficiency:** >175dB FoMs
  - **Med-low speed:** kHz ~ MHz BW

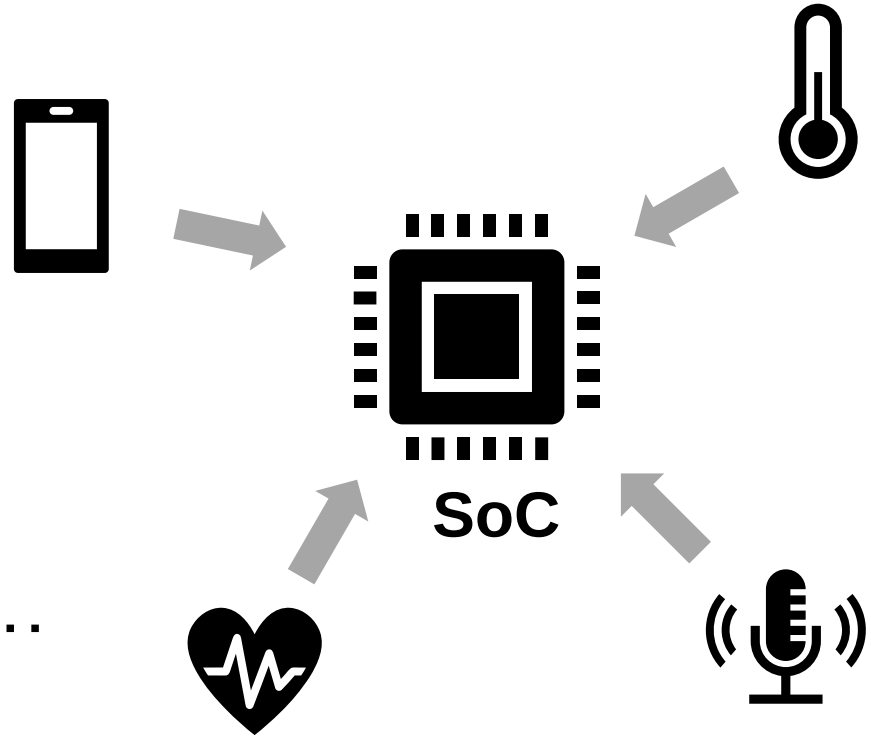
[B. Murmann, “ADC Survey” Jun 2021]



Problem Solved?

- **High SNDR and FoM – Achieved**
- **Higher BW – on the way**
- **But we concern MORE in practice!**
  - Especially for integrated ADC IP

E.g. Wearable devices, IoT, smart sensing…

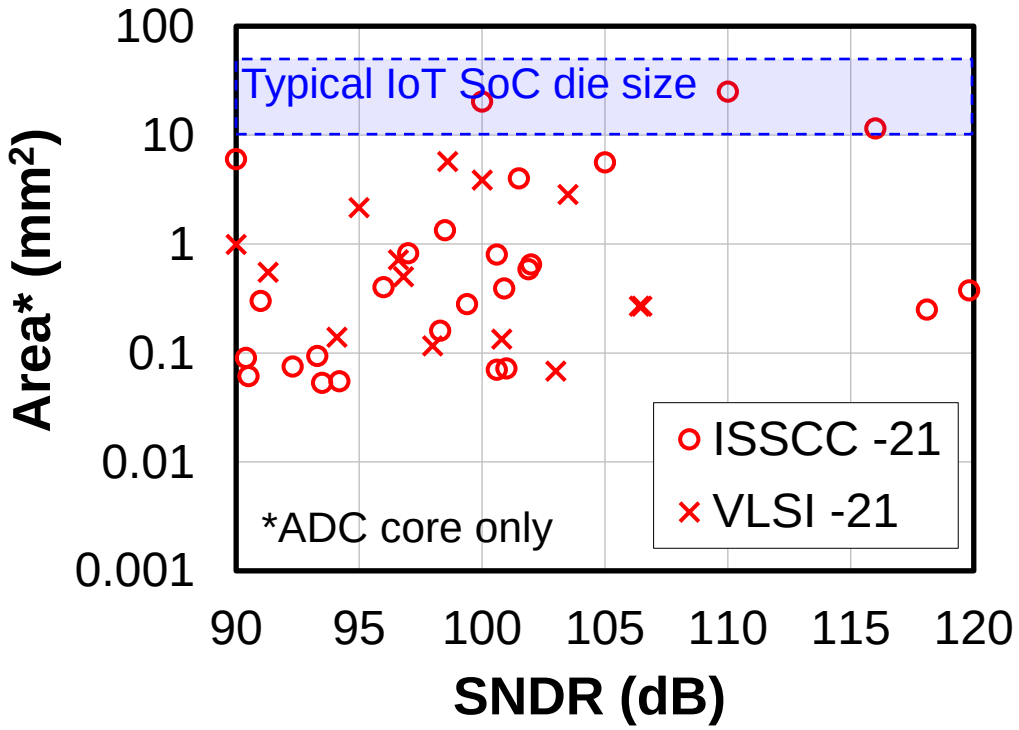


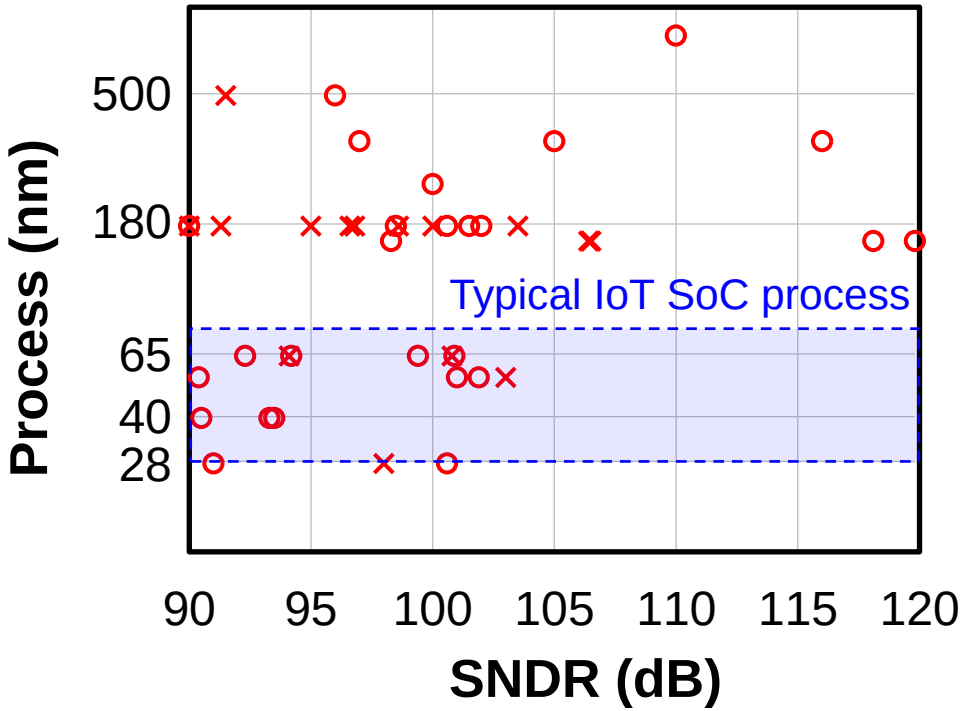
Process and Area Concerns

- **Many advanced high-resolution ADCs are made in old process**
  - And they are large too
- **But SoC prefers advanced process**

Published high-resolution ADCs

[B. Murmann, "ADC Survey" Jun 2021]

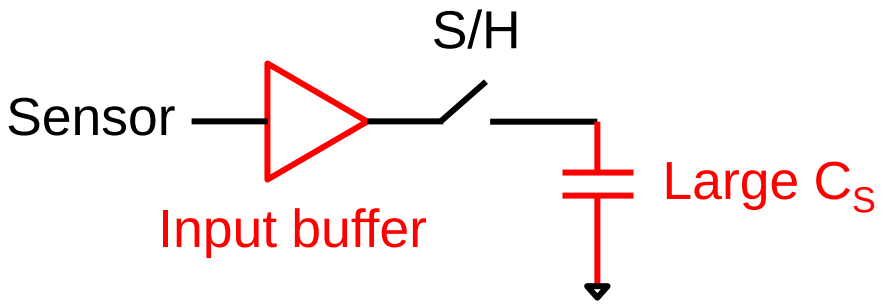


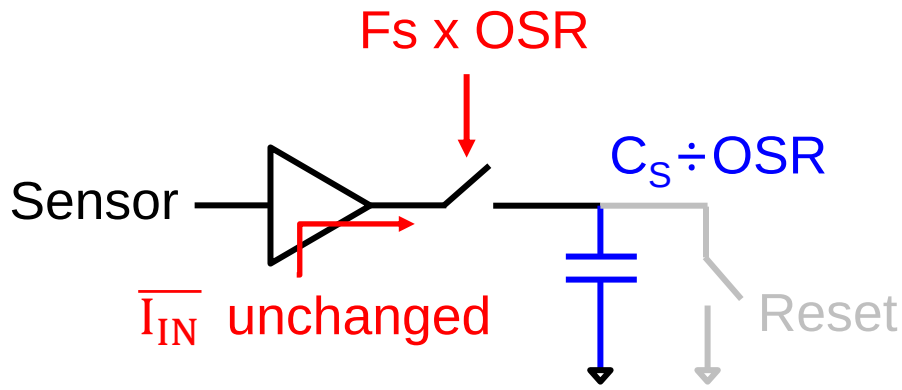


Driving Effort

- **Driving high-resolution Nyquist ADC is a big challenge**
  - Cs is large for low KT/C

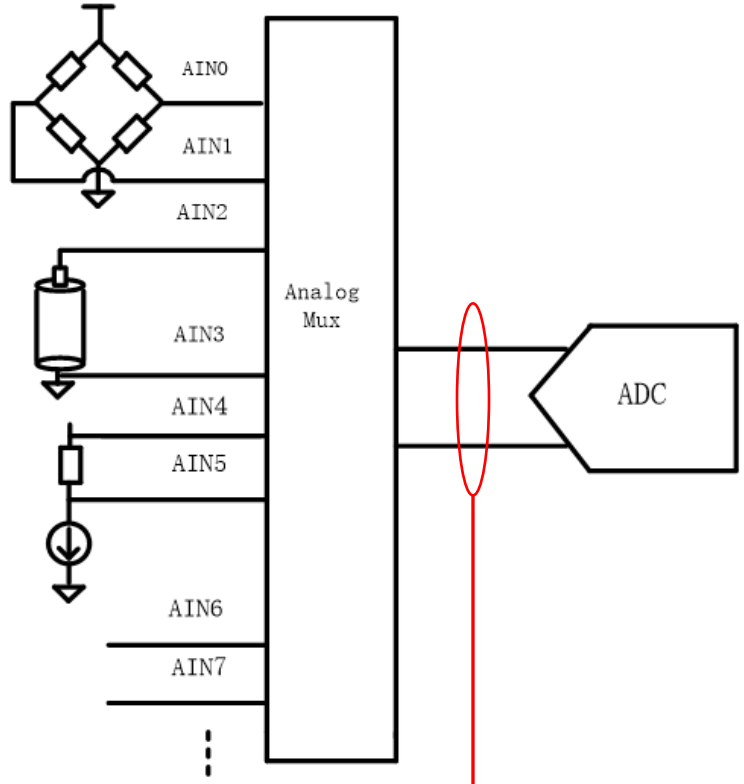
- **Oversampling does not fully relax driving effort**
  - Need to charge Cs faster

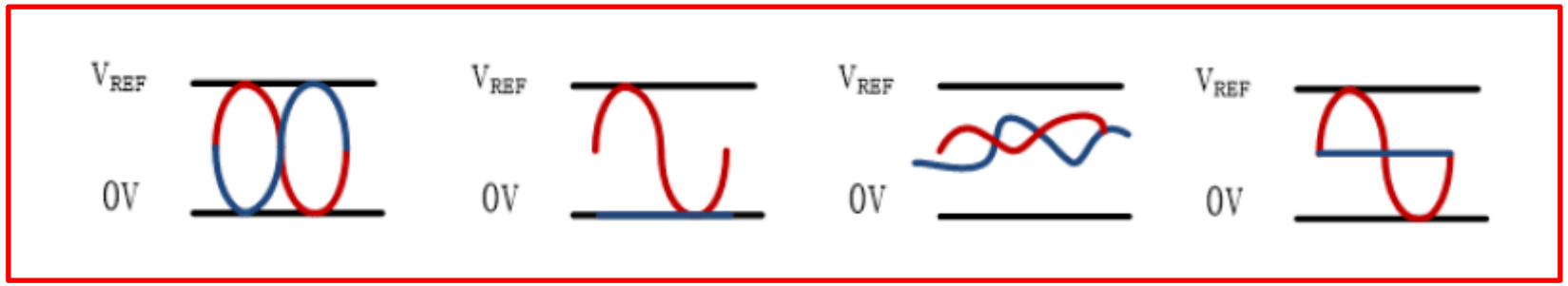




Nyquist And Single-End Capability

- **Many applications need a “Nyquist” ADC**
  - Support single-shot conversion
  - Support multiplexing
- **Single-ended capability is also desired**
  - Compatible with various input formats
  - i.e., a high full-scale CMRR





And More …

- **Decoupling**
  - Many high-resolution ADCs heavily rely on large decaps
  - Typically for stabilizing / denoise references
  - E.g. SAR ADC
- **Calibration and trimming**
  - Foreground calibration / trimming increases testing cost
  - Background calibration / DEM increases P/A cost
- **PVT robustness**
  - Sometimes ignored by academic designs

…

The Complete Wish List

- High SNDR and FoM → ✓ Lots of solutions

Practical Features:

- Advanced process compatible → ✗ OTA, high swing -> more digital?
- Low area
- Easy driving → ✗ SAR / pipe -> oversampling? KT/C cancel?
- Nyquist capable → ✗ DSM -> Incremental?
- Single-ended capable
- Easy decoupling → ✗ CT-DSM ?
- Calibration / trimming free
- PVT Robust → ✗ Open loop based ?

…

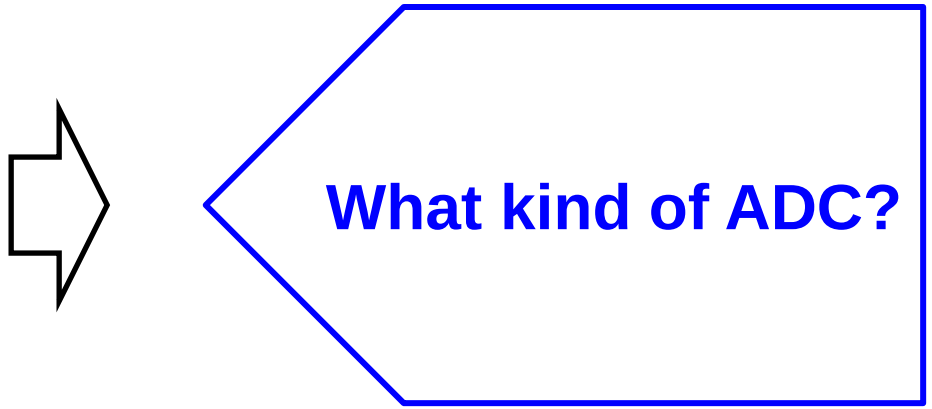
The Complete Wish List

- ✓ High SNDR and FoM

Practical Features:

- ✓ Advanced process compatible
- ✓ Low area
- ✓ Easy driving
- ✓ Nyquist capable
- ✓ Single-ended capable
- ✓ Easy decoupling
- ✓ Calibration free
- ✓ PVT Robust

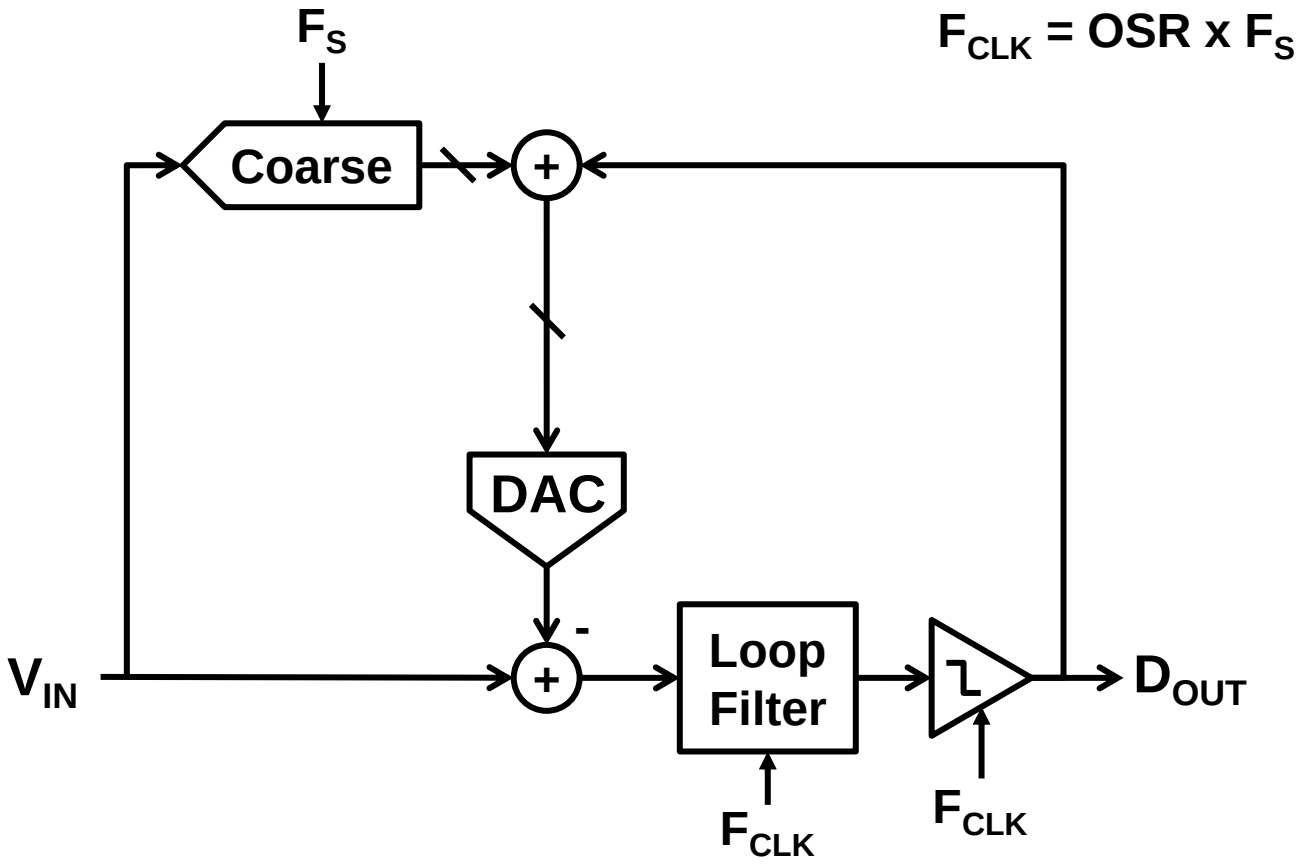
…



[Y. Chae, ISSCC' 13]

The "Zoom" Framework

- **Slow coarse stage + single-bit DSM**
  - ✓ Effectively multi-bit
  - ✓ Inherent linear DSM
  - ✓ Low DAC toggle rate
  - ✓ Small input to LF
  - ✗ DAC mismatch unsolved
  - ✗ Only works for DC
  - ✗ Massive SC input sampling



Mismatch Error in DAC

- **Mismatch error in DAC brings nonlinearity**

Thermometer DAC (2bits)

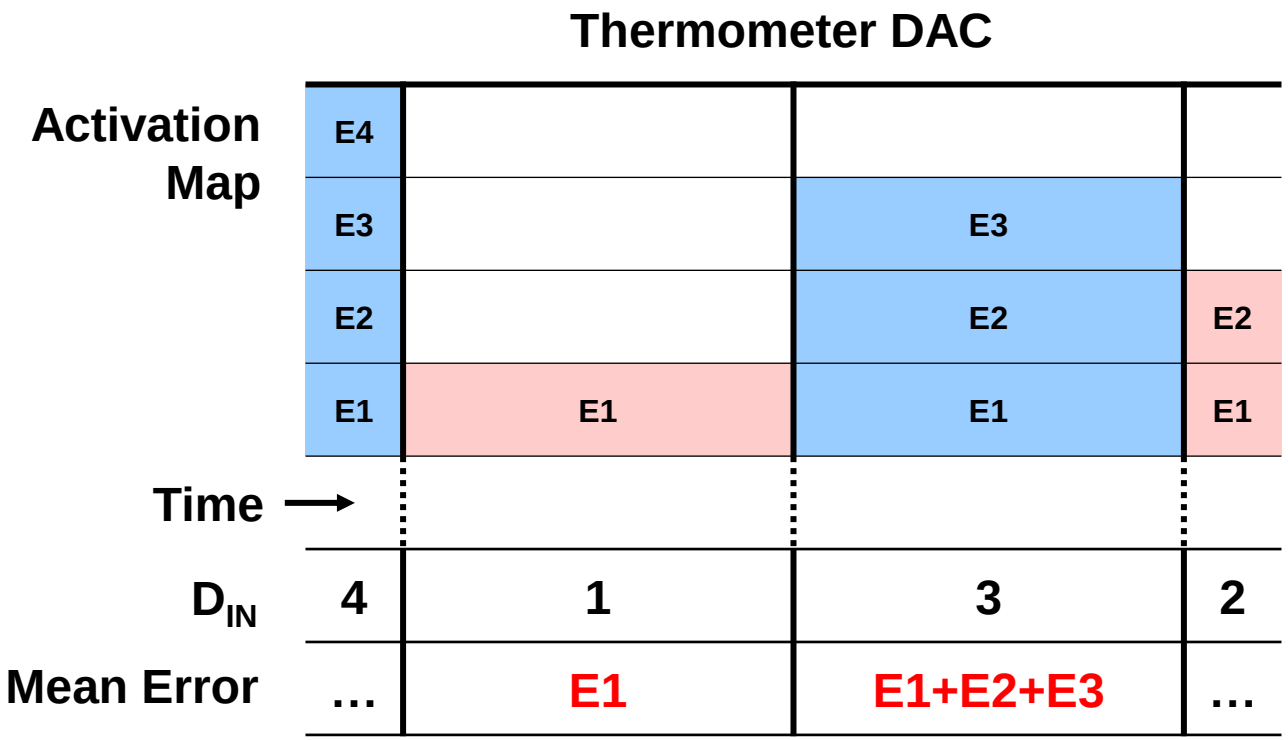
Activation Map				
	E4			
	E3		E3	
	E2		E2	E2
	E1	Mismatch Error (E1)	E1	E1
Time →				
D_{IN}	4	1	3	2
Mean Error	…	E1	E1+E2+E3	…

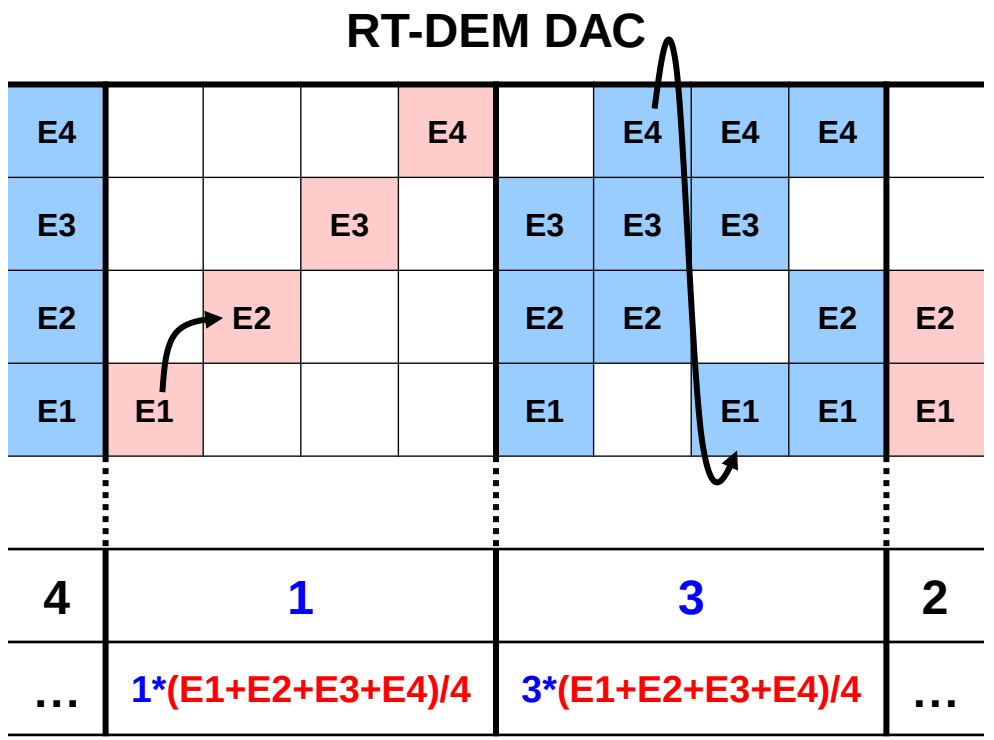
Error $\not\propto$ D_{IN} ⇨ Distortion

[E. Tuijl, ISSCC' 04]

The "Real Time"(RT) DEM

- **Circulate the elements step-by-step for a complete round**





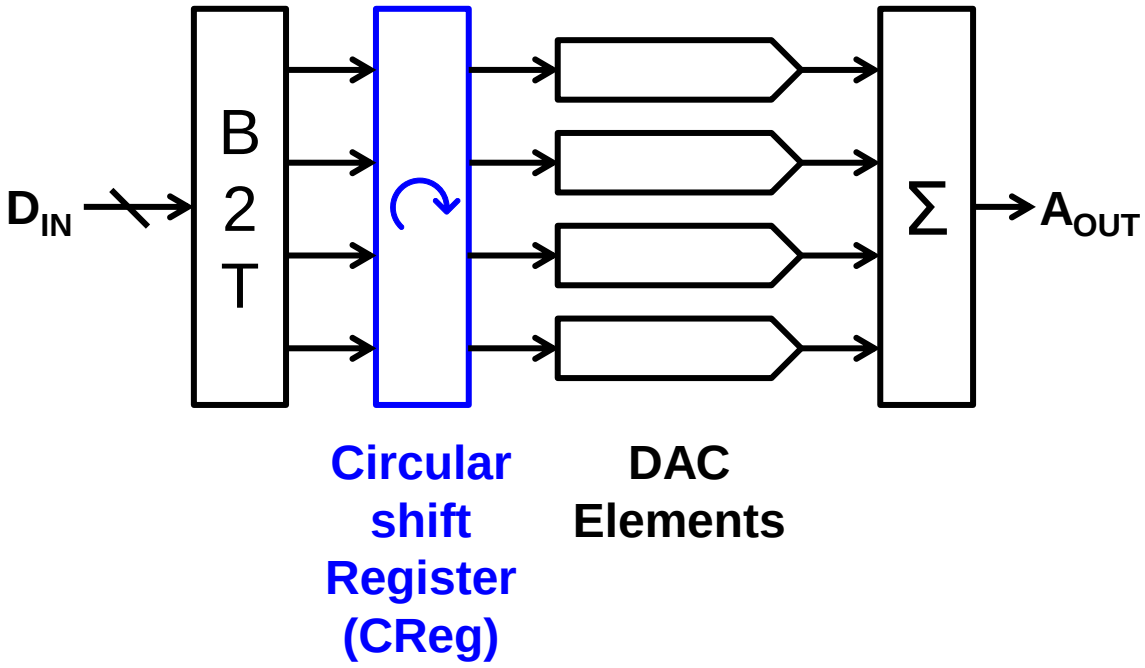
Error ~~∝~~ D_{IN} ⇨ Distortion

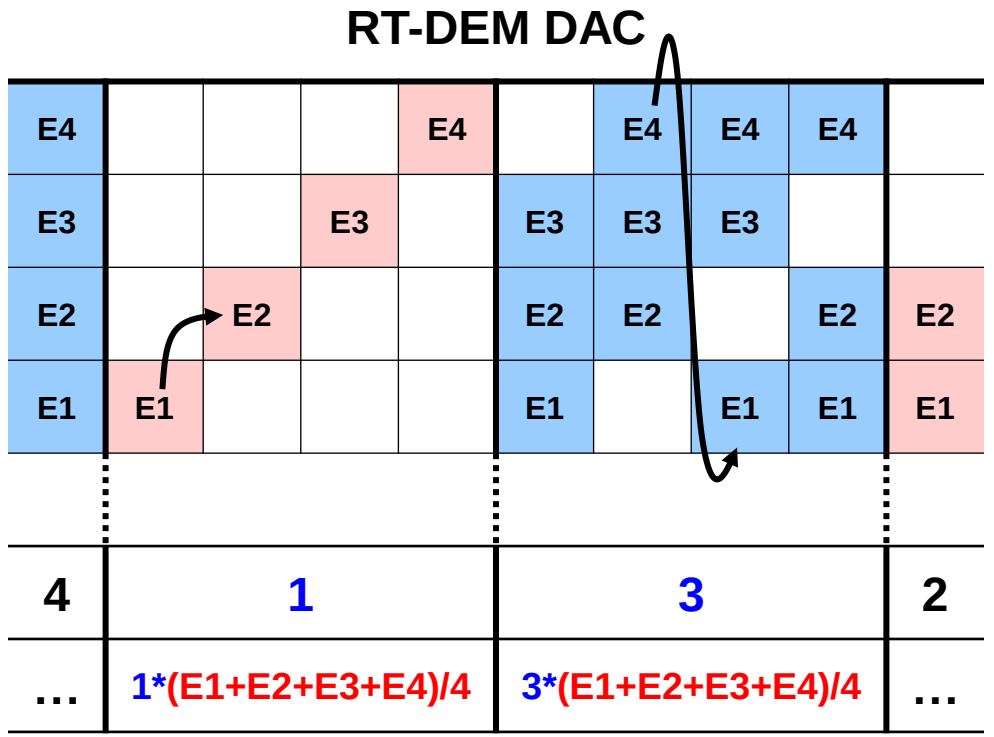
Error ∝ D_{IN} ⇨ Linear gain error

[E. Tuijl, ISSCC' 04]

The "Real Time"(RT) DEM

- ✓ Remove mismatch **completely**
- ✓ Simple implementation





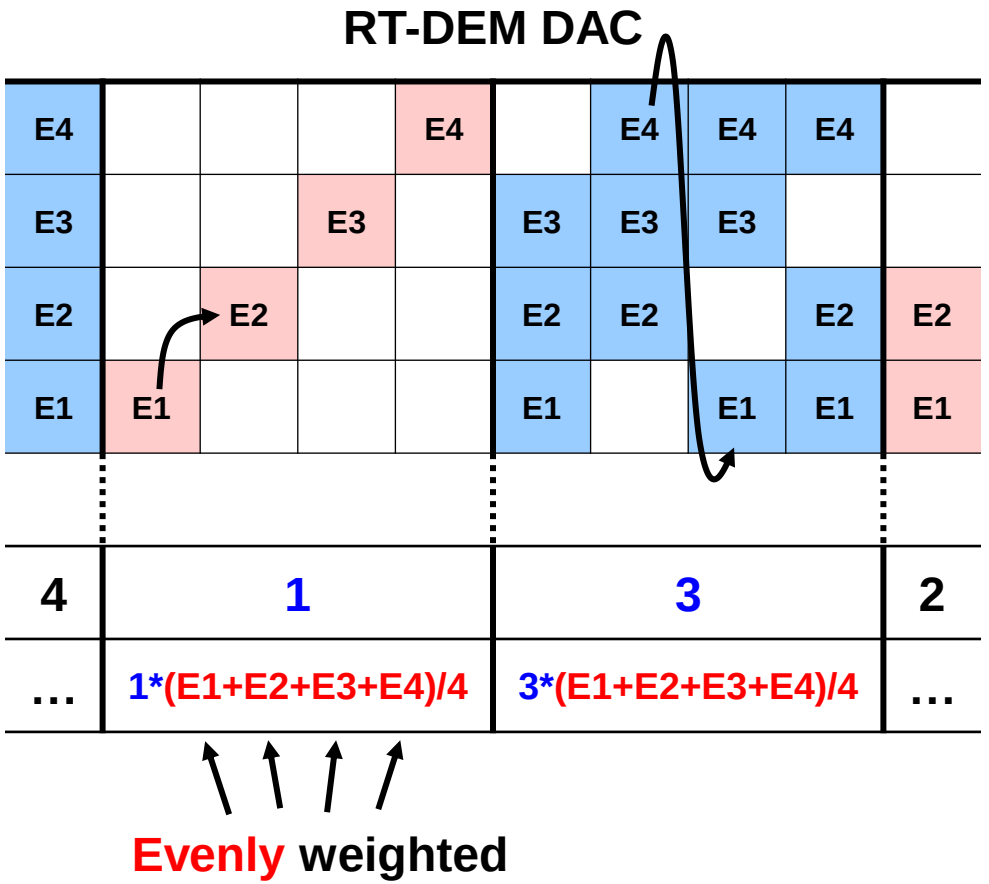
Error ∝ D_{IN} ⇨ Linear gain error

[E. Tuijl, ISSCC' 04]

The "Real Time"(RT) DEM

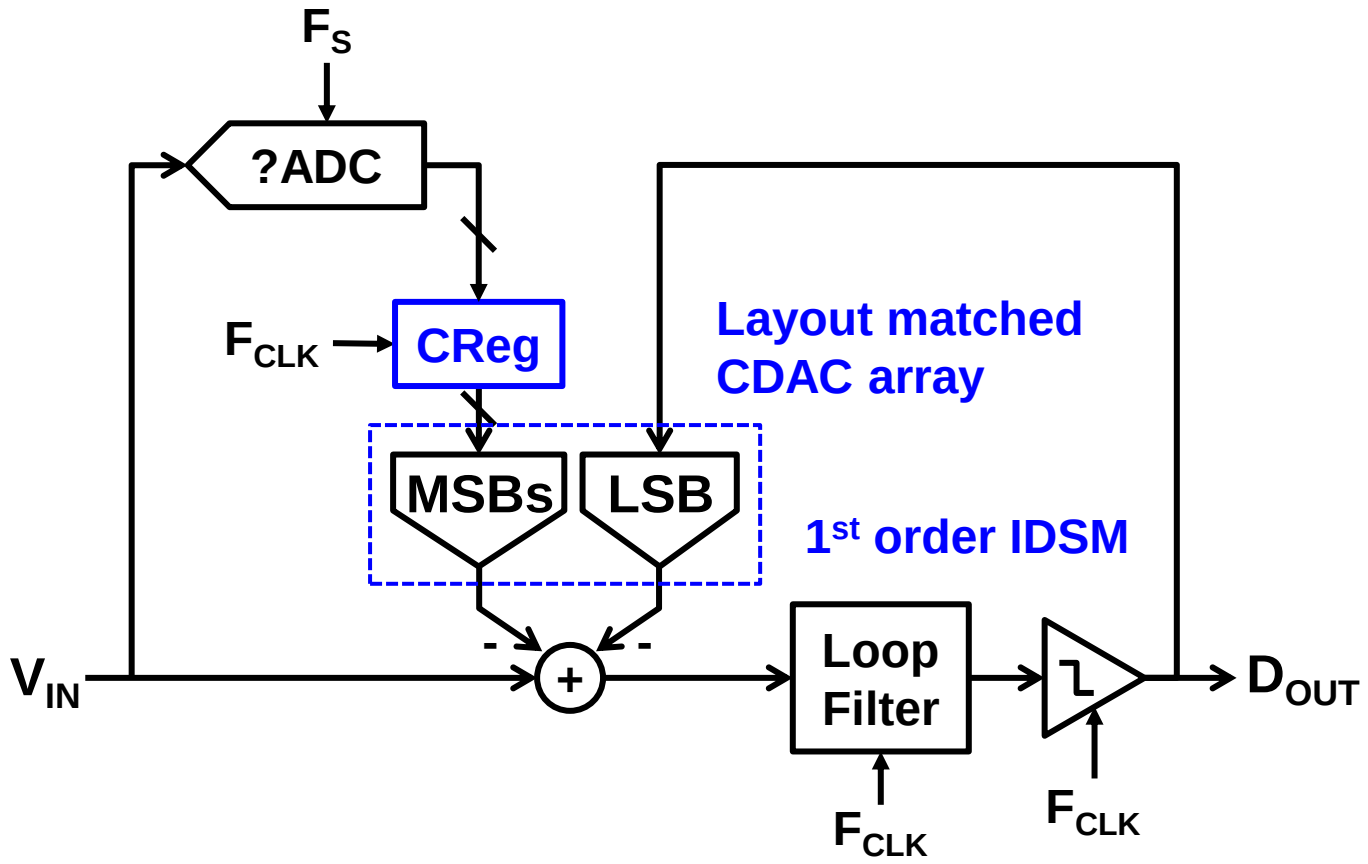
- ✓ **Remove mismatch completely**
- ✓ **Simple implementation**
- **Limitations**
  - High OSR
  - 1st-order IDSM

} **OK for advanced process**



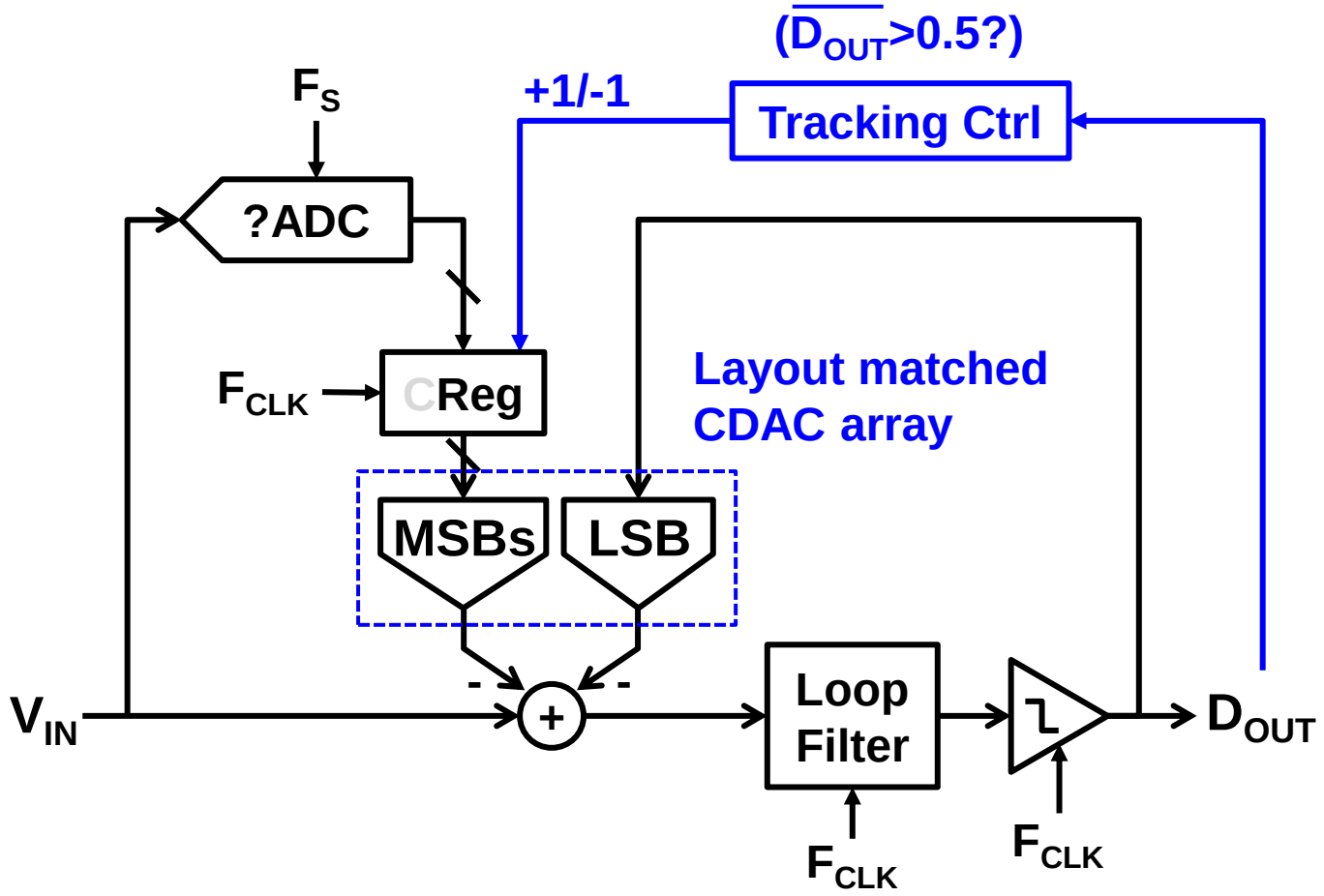
Decoupled Stages with RT-DEM

- ✓ Simple hardware
- ✓ Completely remove mismatch
- ✓ Low toggle rate
- ✓ Code independent ripple
- ? Cannot track AC



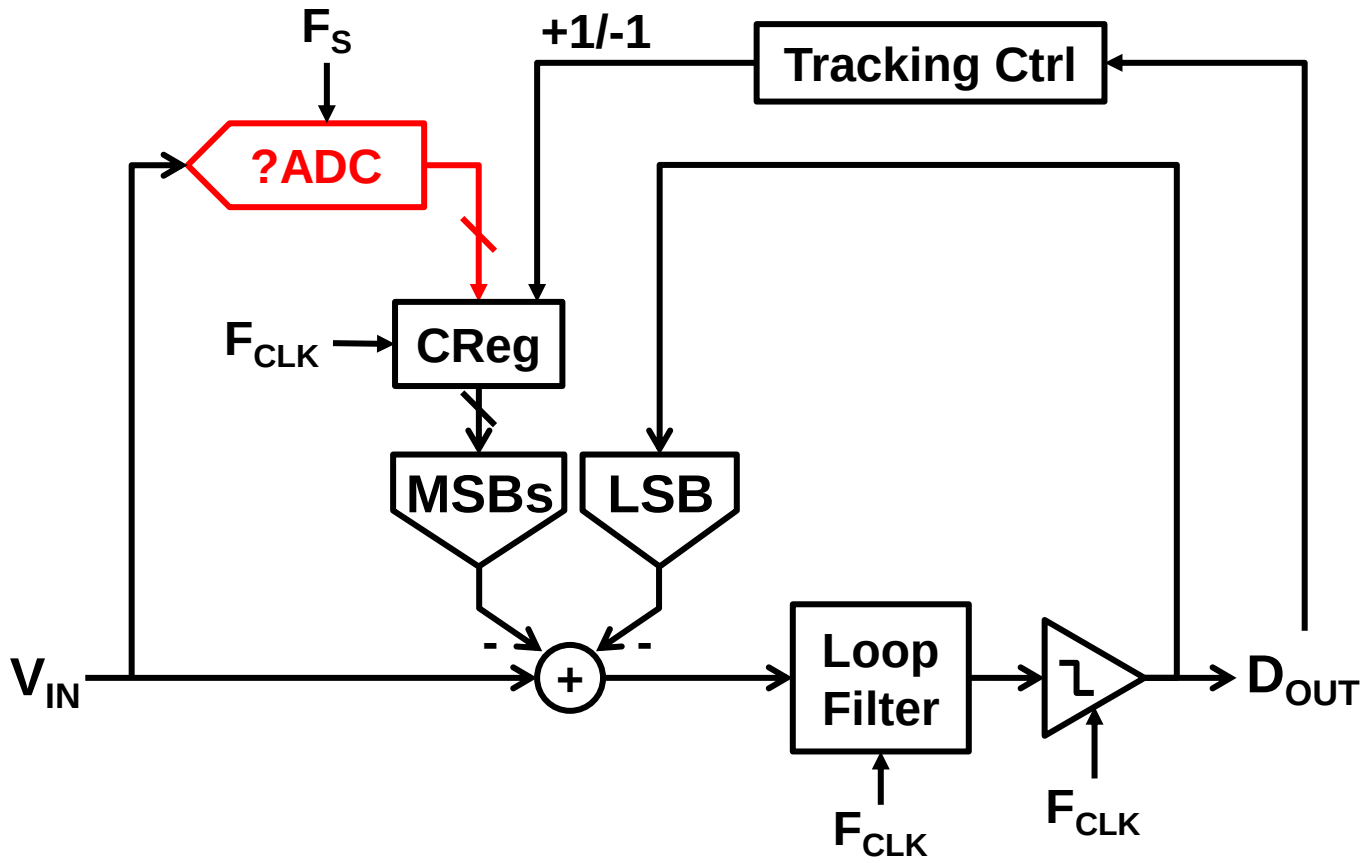
Introduce Tracking Mechanism

- ✓ Simple hardware
- ✓ Completely remove mismatch
- ✓ Low toggle rate
- ✓ Code independent ripple
- ✓ Tracks input
- ✓ Gain calibration free



Implement Coarse ADC

- ✓ Simple hardware
- ✓ Completely remove mismatch
- ✓ Low toggle rate
- ✓ Code independent ripple
- ✓ Tracks input
- ✓ Gain calibration free
- ? Needs complicated B2T



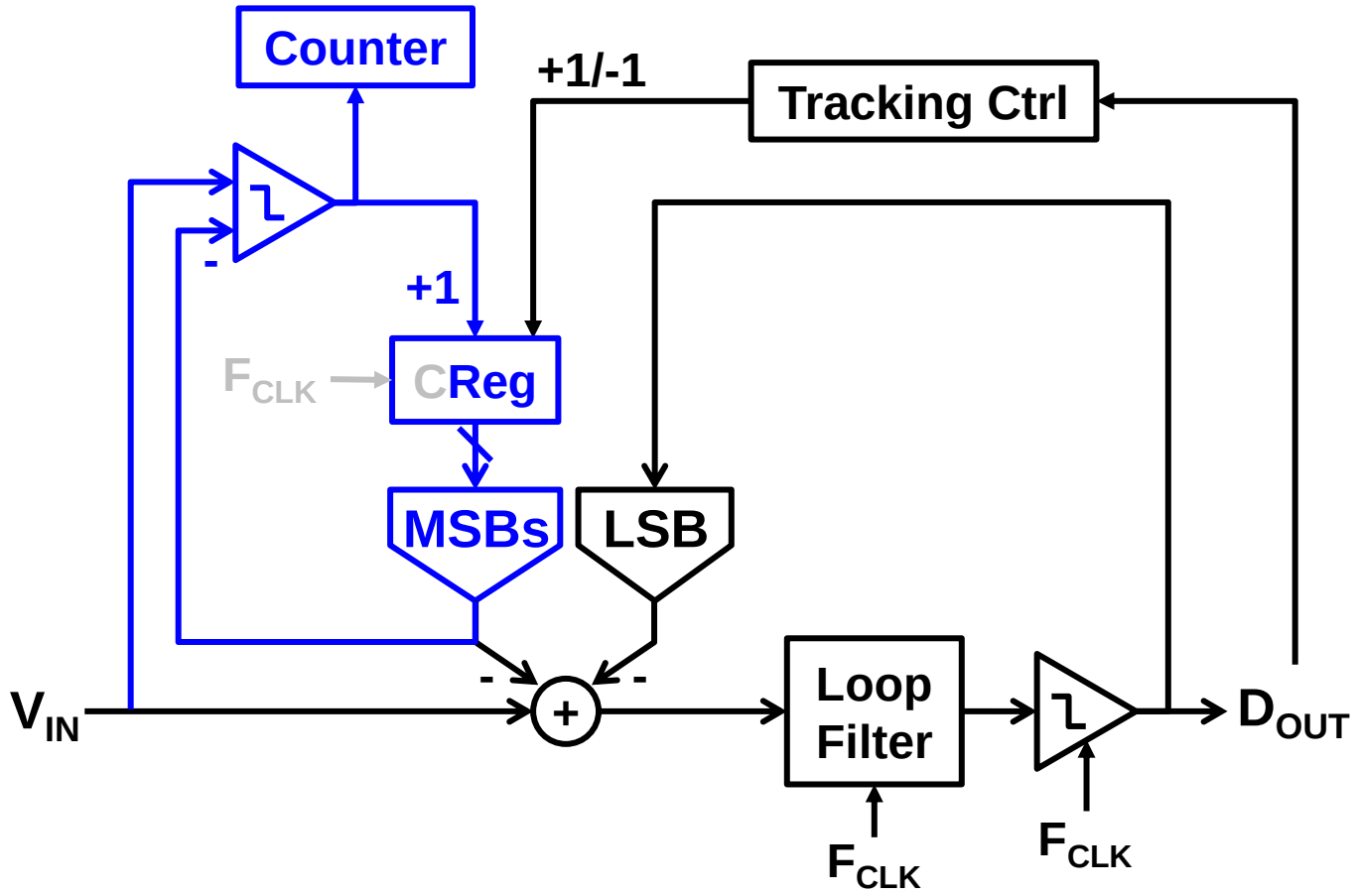
- What is the simplest ADC providing “thermometer” output?

Simplest – Counting ADC

- **Ramp DAC's output till V_{IN}**
- **Count the steps of ramping**

✓ **Reusing the DEM and DAC**

- ✓ No B2T!
- ✓ Low power
- ✓ Compact

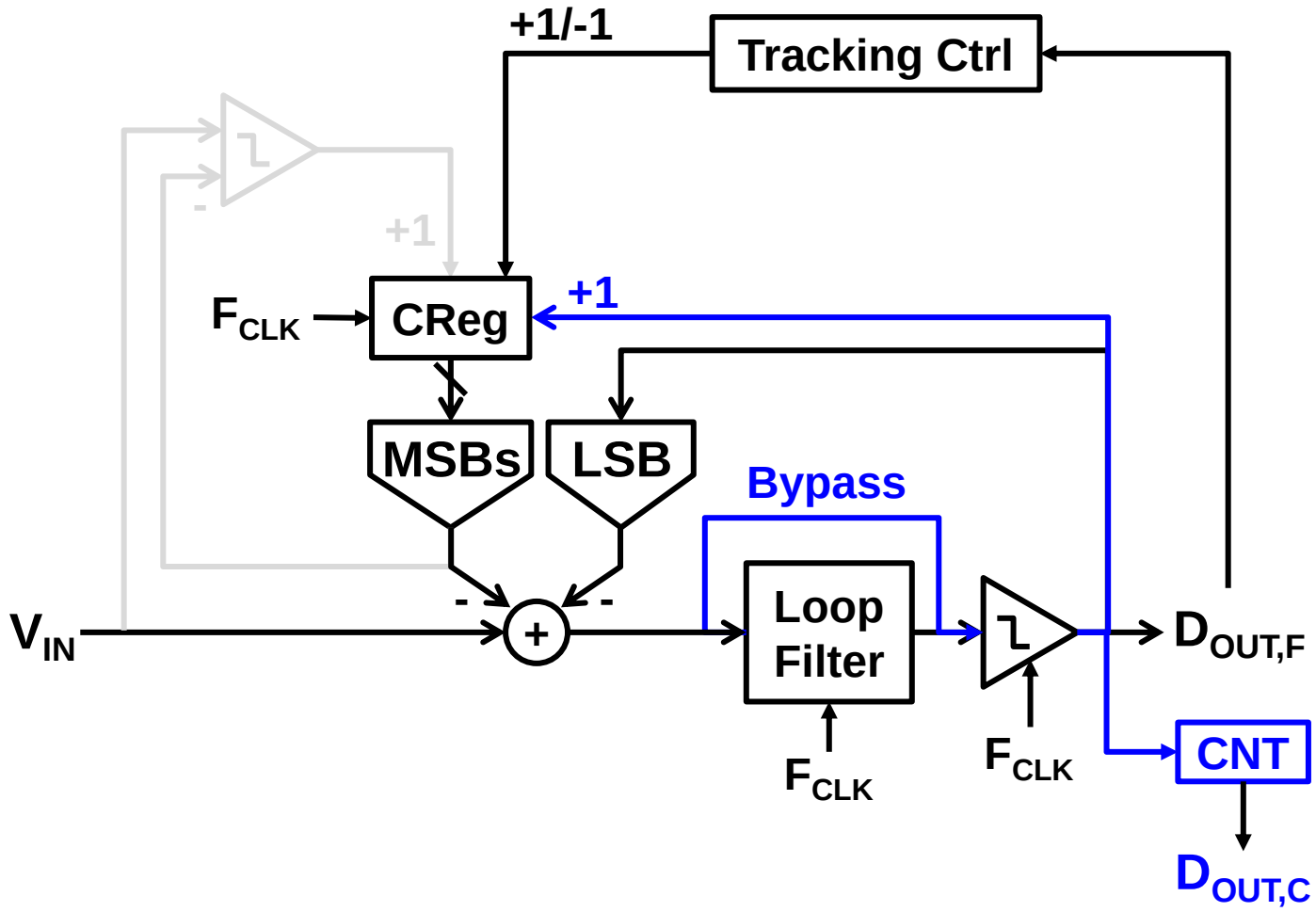


Even Simpler – Comparator Reuse

- **Ramp DAC's output till V_{IN}**
- **Count the steps of ramping**

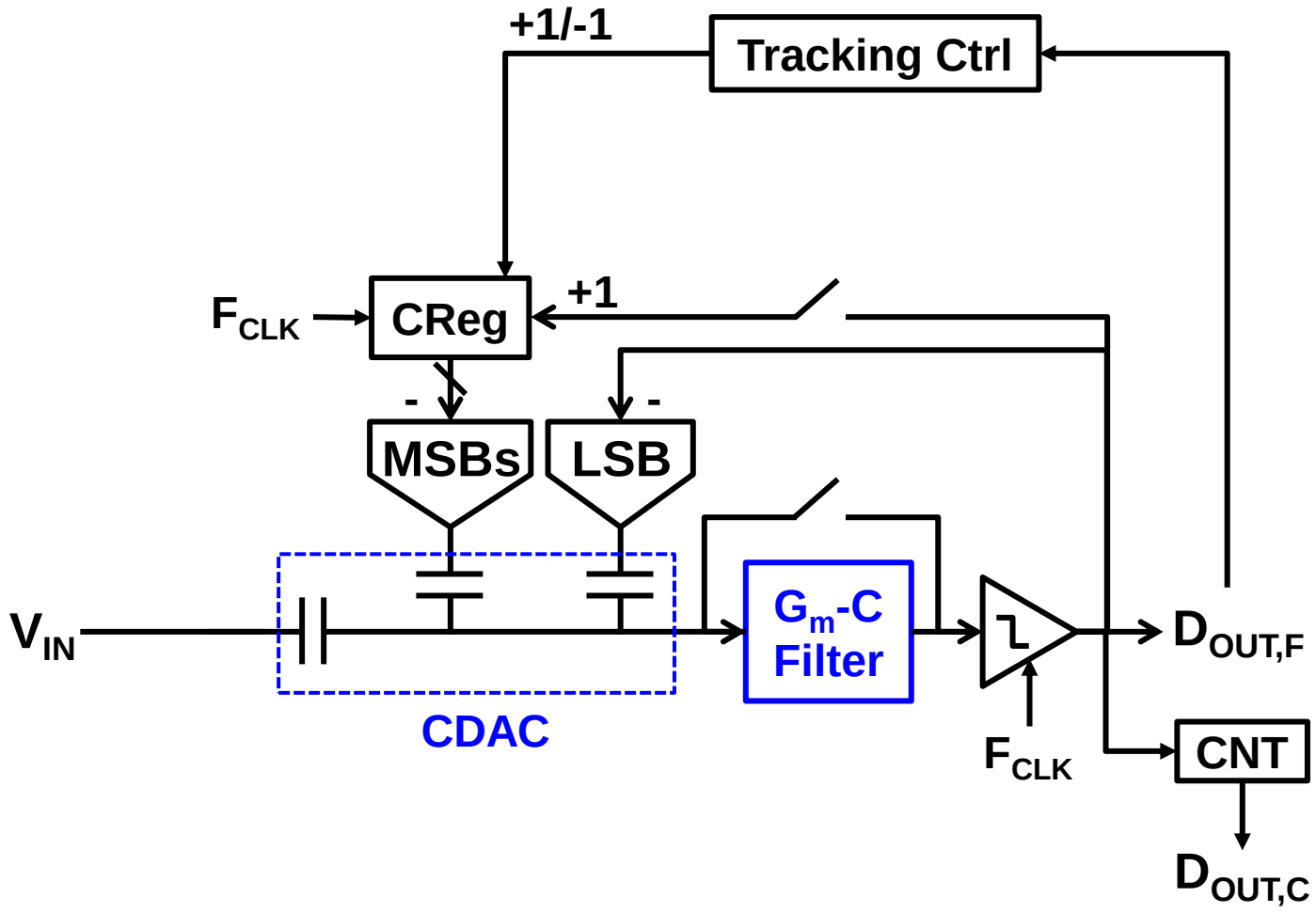
✓ **Reusing all hardware**

- ✓ No B2T!
- ✓ Low power
- ✓ Even more compact!



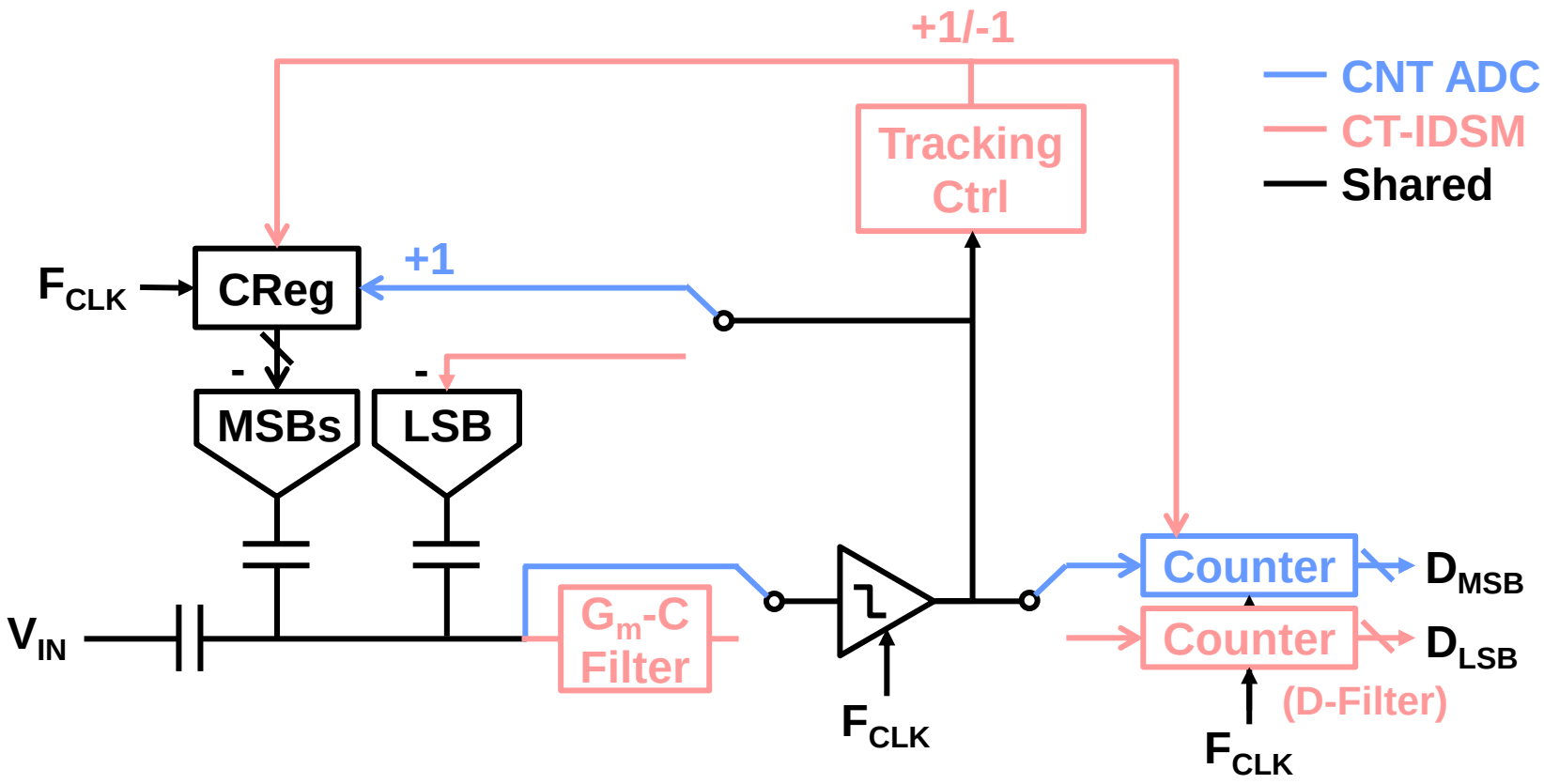
Switch to Continuous-Time

- **Gm-C loop filter (integrator)**
  - ✓ Fast, settling free
  - ✓ High efficiency
  - ✓ Linearity relaxed by small input
  - ✓ Low swing - scaling friendly
- **Cap-coupled input**
  - ✓ Easy driven
  - ✓ kT/C noise free

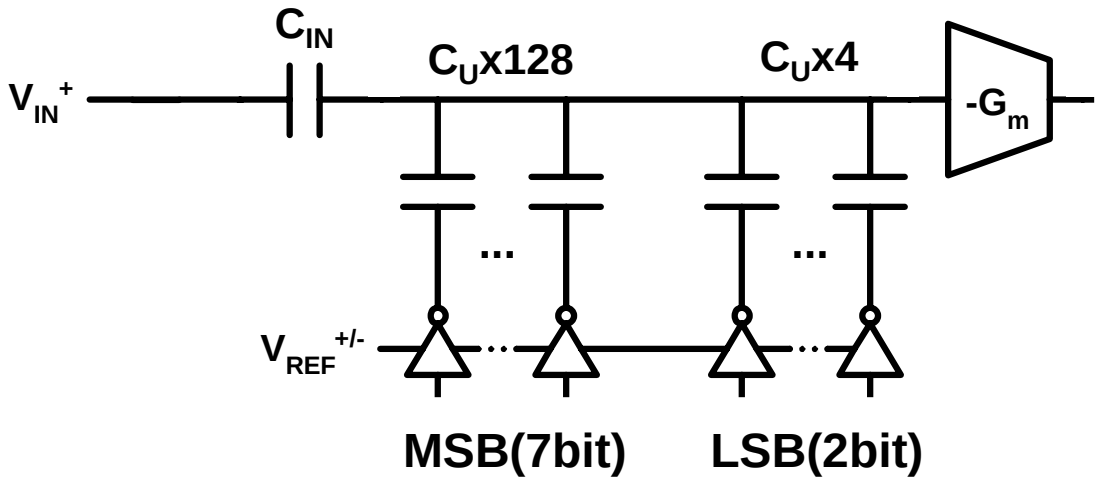


“Zoom of Incremental + Counting” (ZIC)

- ✓ High SNDR
- ✓ Good scalability
- ✓ Small and simple
- ✓ Easy driving
- ✓ Stable Vref ripple
- ✓ Nyquist capable
- ✓ Calibration free
- ✓ PVT Robust



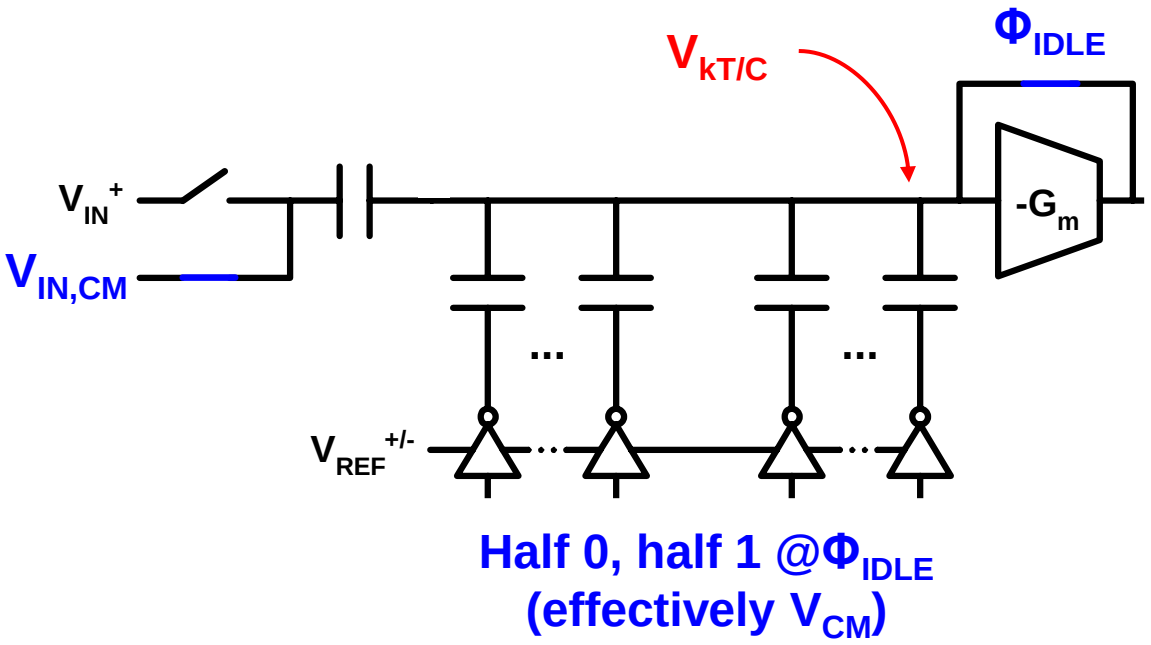
Input Network Concern



- Cap coupling – easy driving
  - ✗ Cannot accept DC input

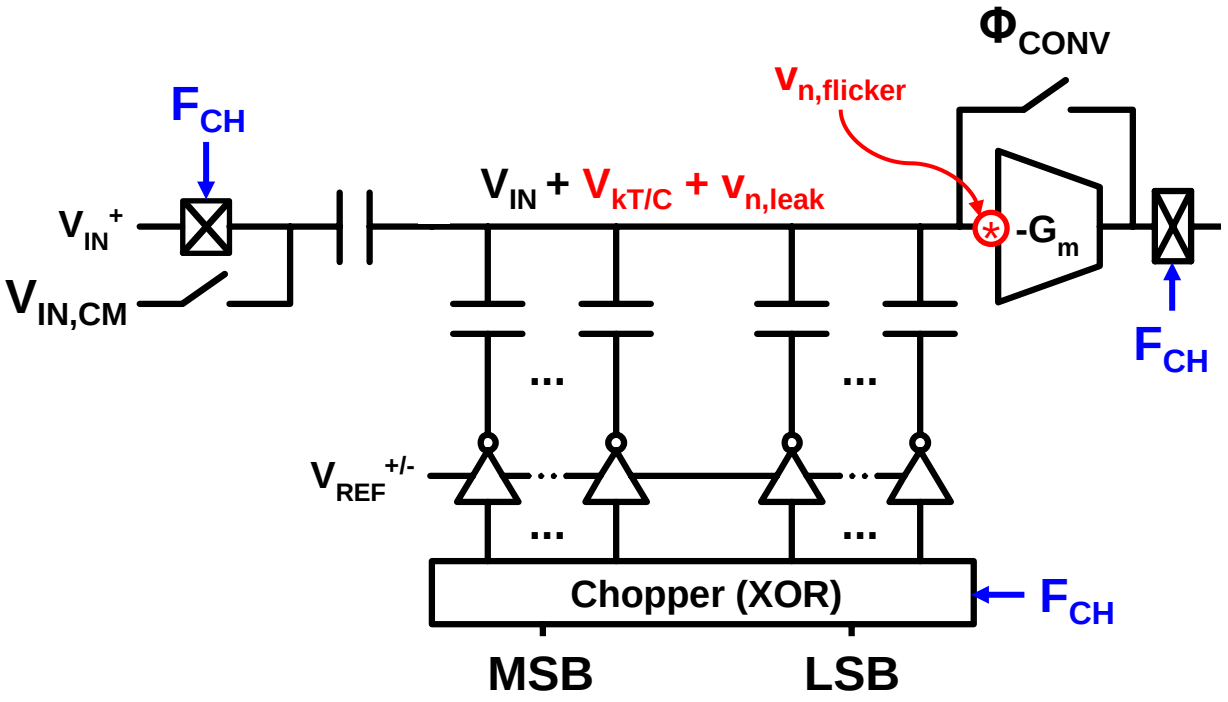
$C_U = 12.5fF$
$C_{IN} = 132C_U$

Input Network Concern



- Cap coupling – easy driving
- Reset during idle
  - ✓ Reset to $V_{IN,CM}$ gives great CMRR
  - ✗ Induce kT/C noise

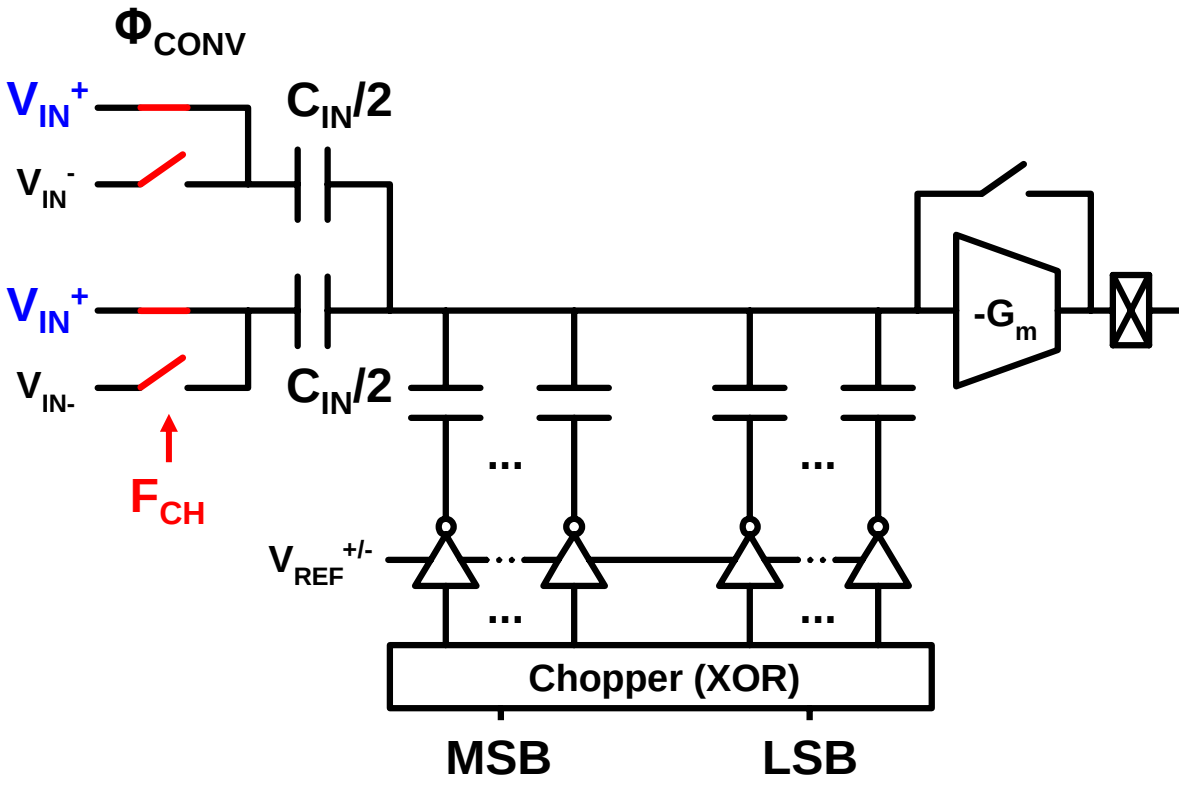
Input Network Concern



- Cap coupling – easy driving
- Reset during idle
- Apply chopping – kT/C is DC error
  - ✓ Also suppress flicker noise and leakages

[H. Wang, ISSCC' 17]

Input Network Concern



- Cap coupling – easy driving
- Reset during idle
- Apply chopping

➢ $V_{IN,CM} = (V_{IN}^{+} + V_{IN}^{-})/2$

  - Sample both V_{IN} on split C_{IN}
  - Chopping is embedded

Full Schematic

Gm reused as a pre-amplifier

✓ Suppress comparator offset

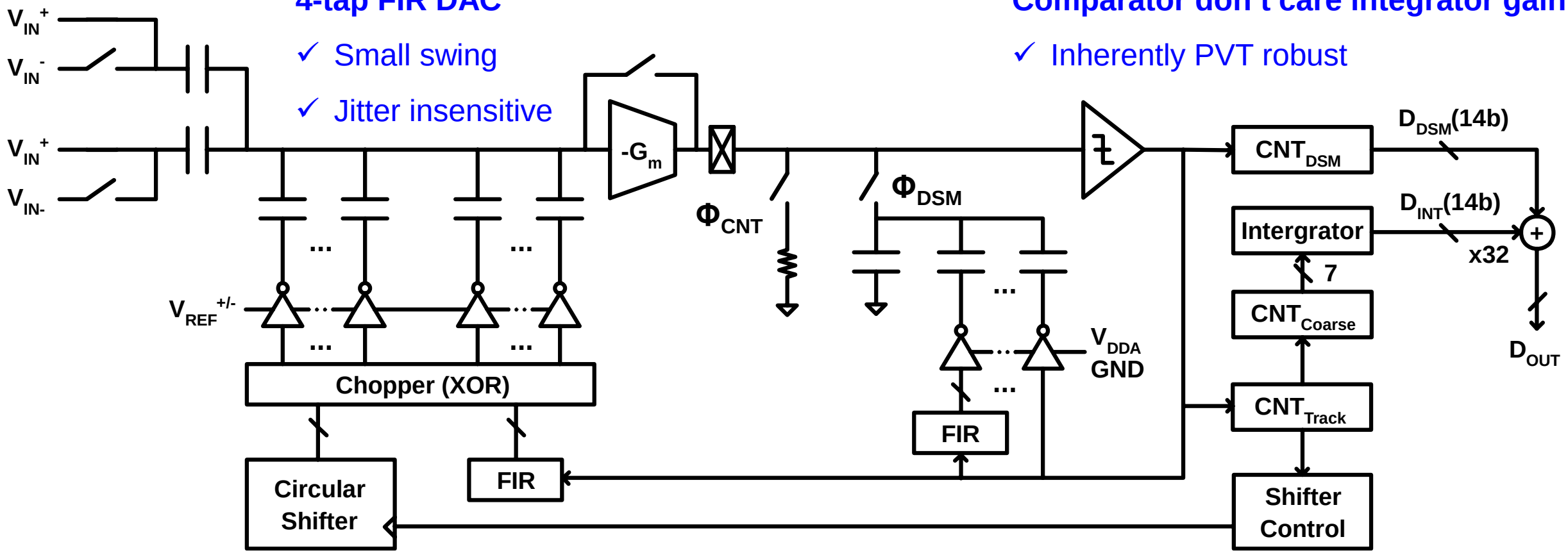
4-tap FIR DAC

✓ Small swing

✓ Jitter insensitive

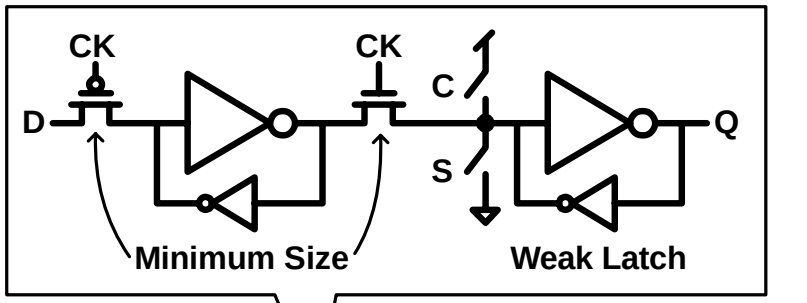
Comparator don't care integrator gain

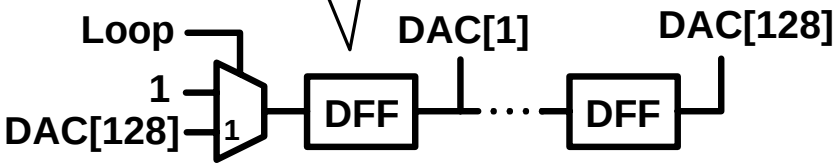
✓ Inherently PVT robust



Dynamic Power Concern

Only two DFFs are flipping at each DEM step





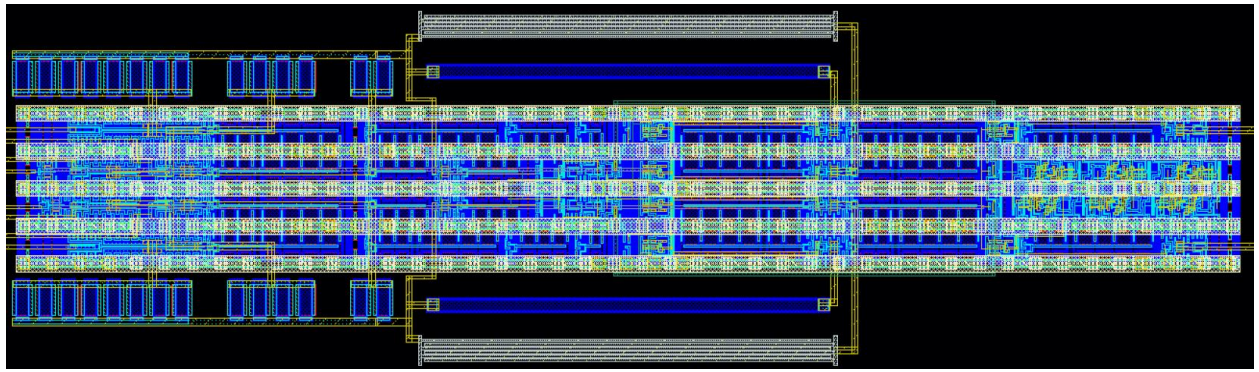
- ✓ **Small gate count → ~100uW @ 500M F_{CLK}**
- ✓ **Can be further reduced in advanced process**

Clock Generation Concern

- **The 500MHz clock sounds costly to generate? - Not really**
  - ✓Loose jitter requirement: 3ps rms for 105dB
  - ✓Loose frequency precision: even ±20% F_{CLK} is tolerable

➢ **A "crappy" free-running relaxation oscillator* is enough**

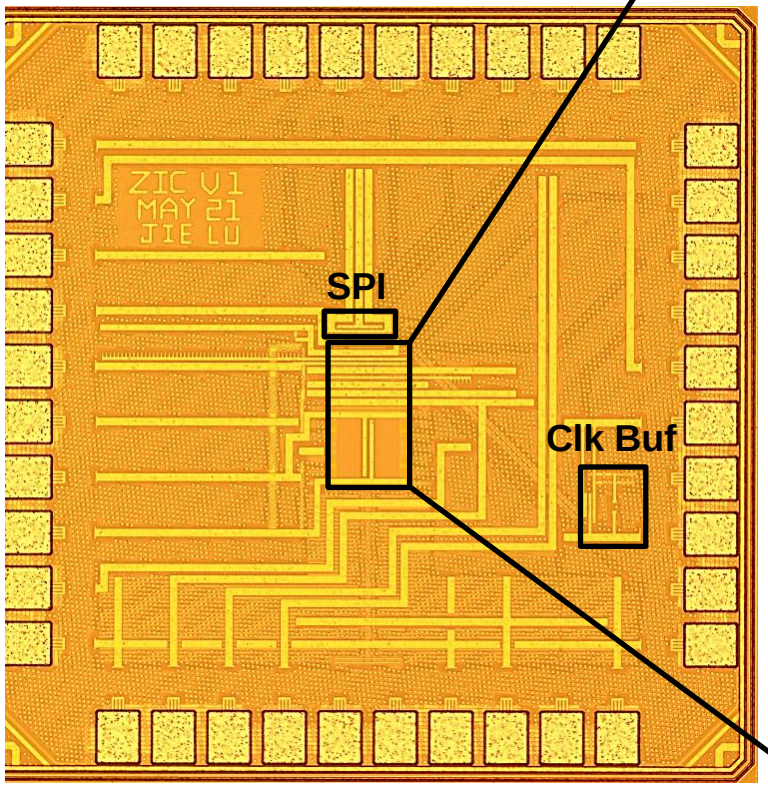
- ~200uW @ 500M (post sim)
- 10x40um
- No trimming needed

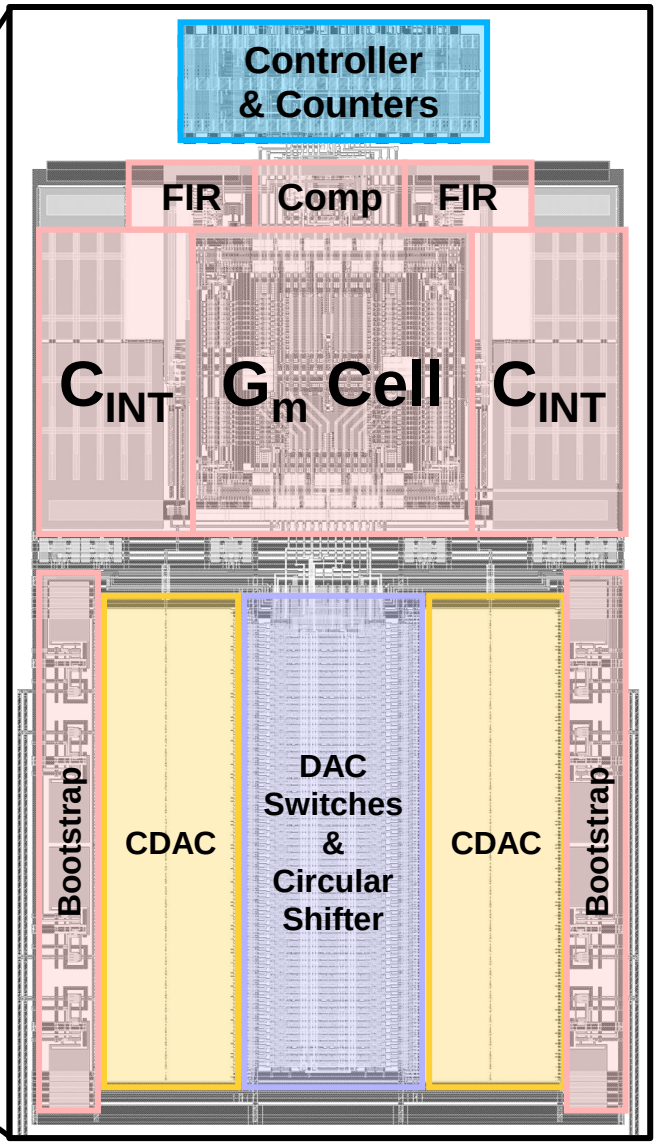


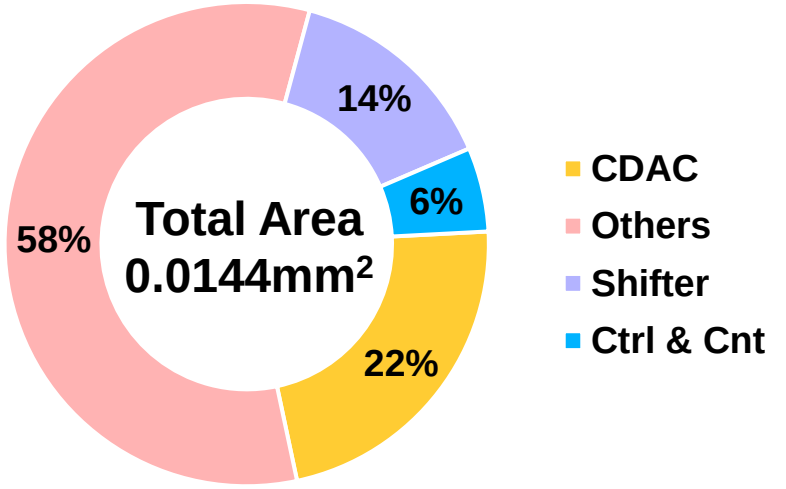
*Not used in actual measurement

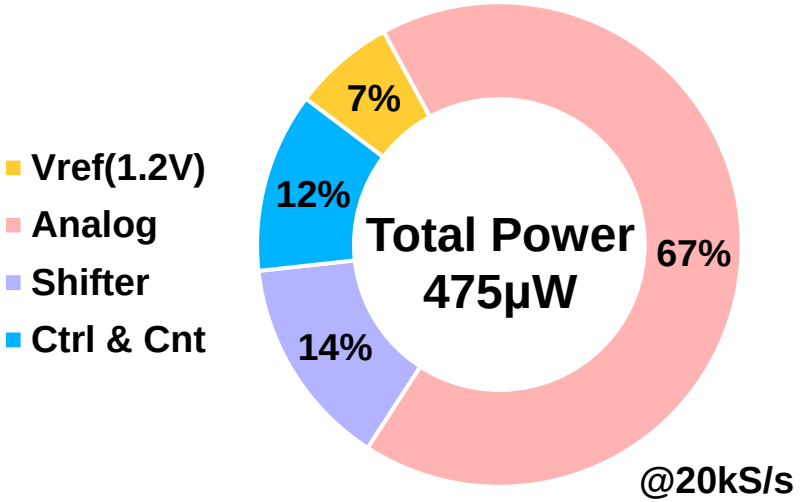
Prototype ADC

- 28nm CMOS
- Core Area: 90x160 um^2



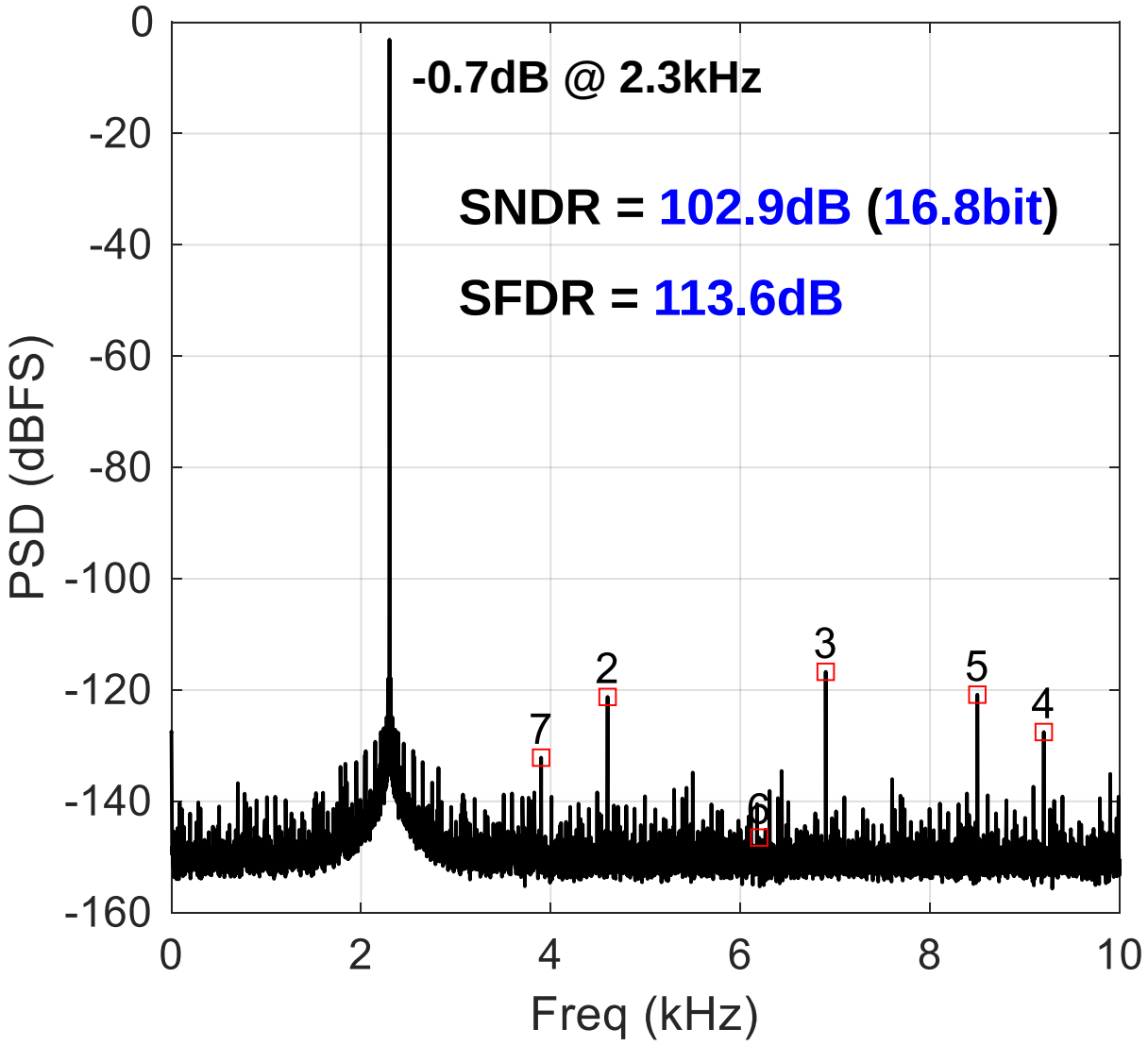


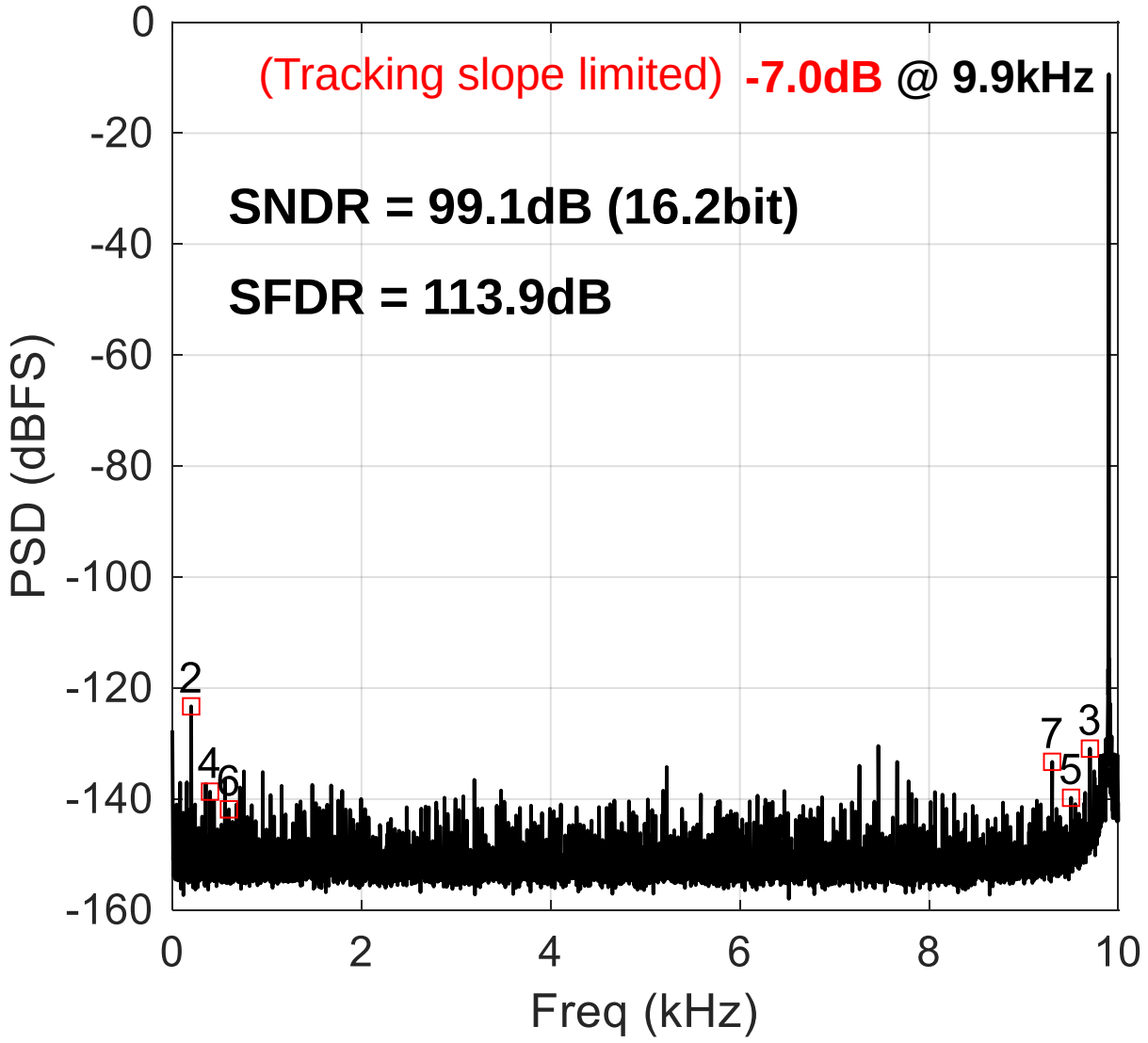




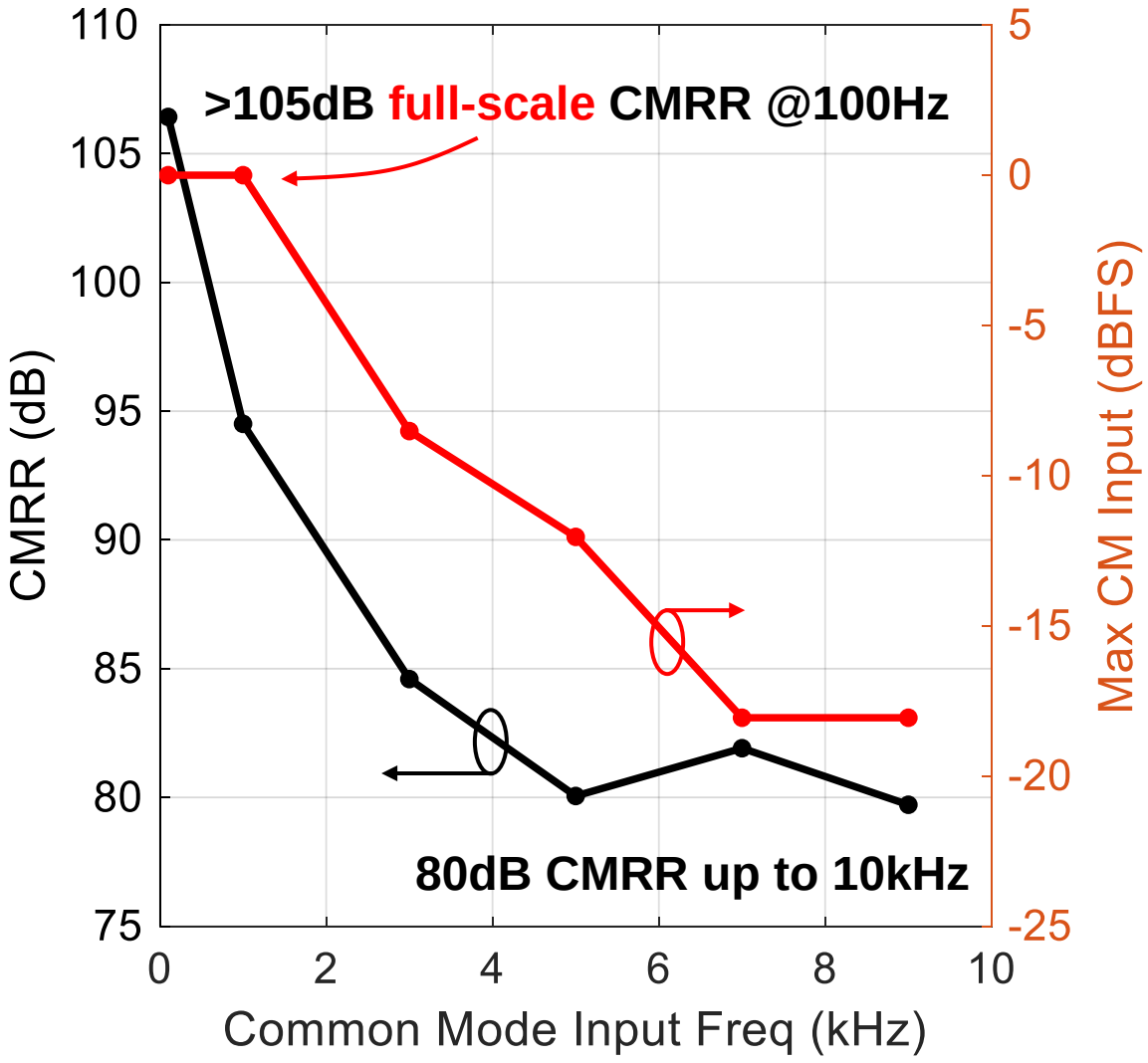
Single-Tone Test @20kS/s

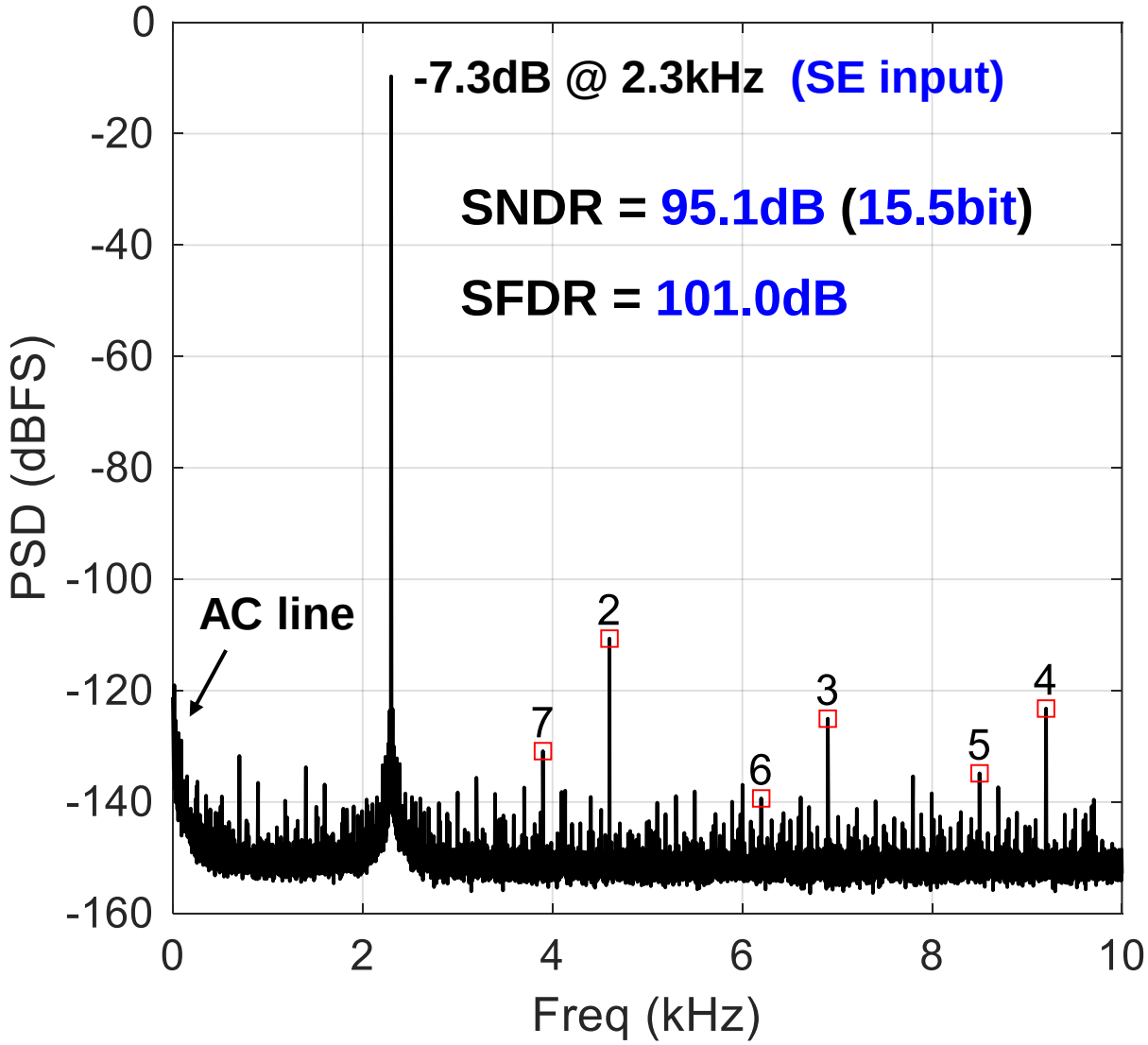
2^{16}-FFT, 16x Averaged



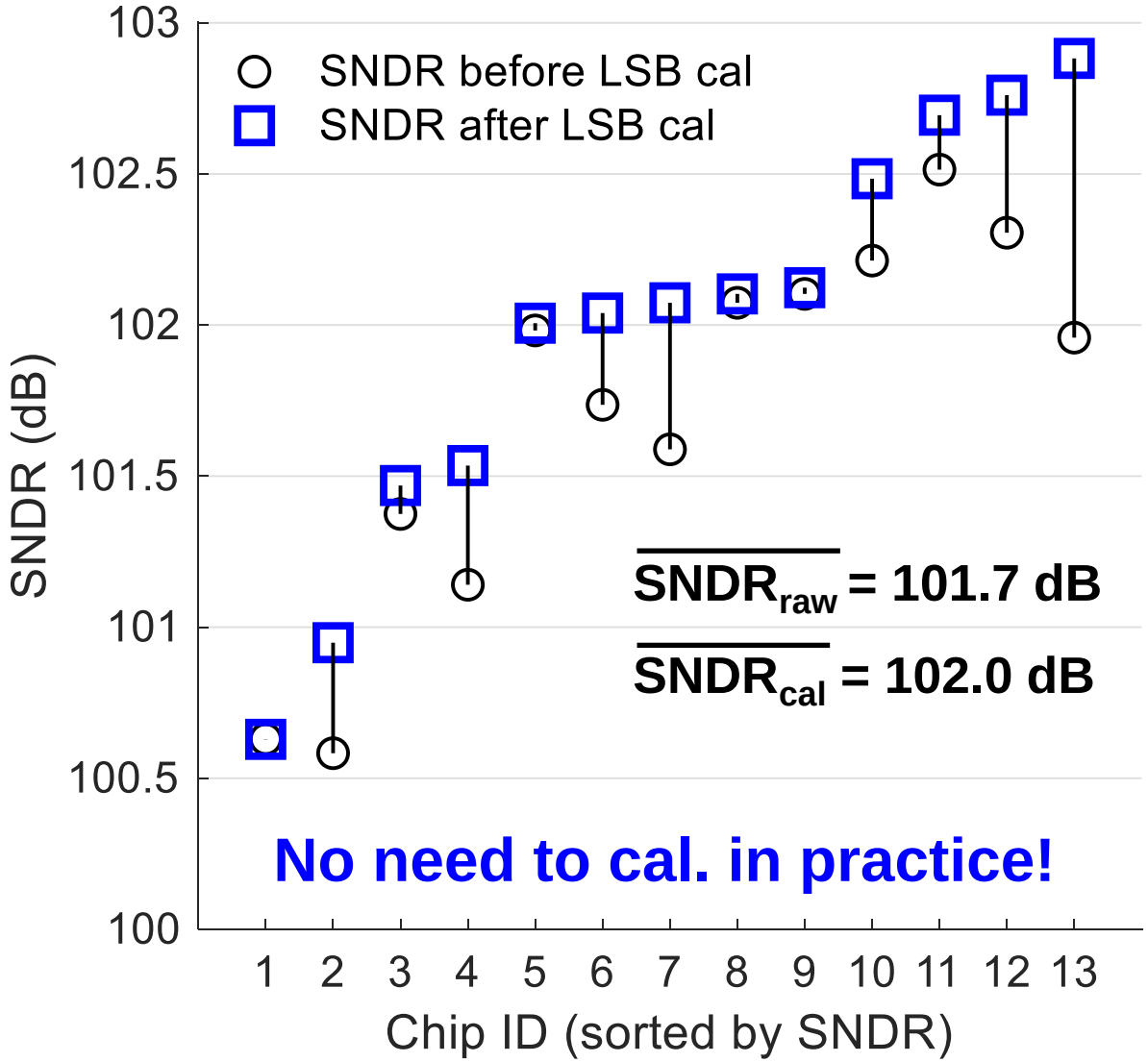


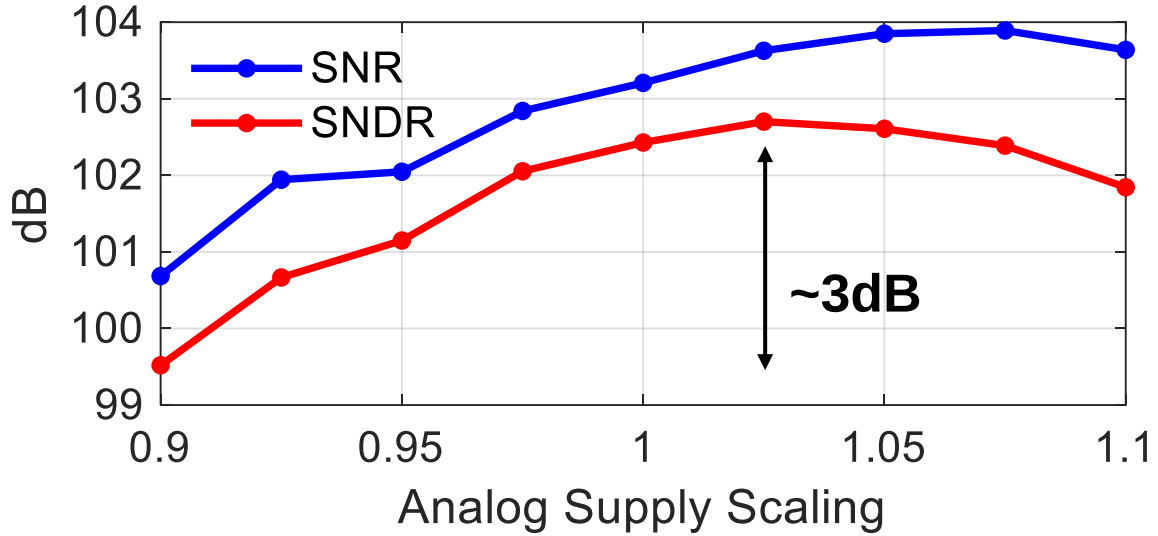
CMRR and Single-Ended Input

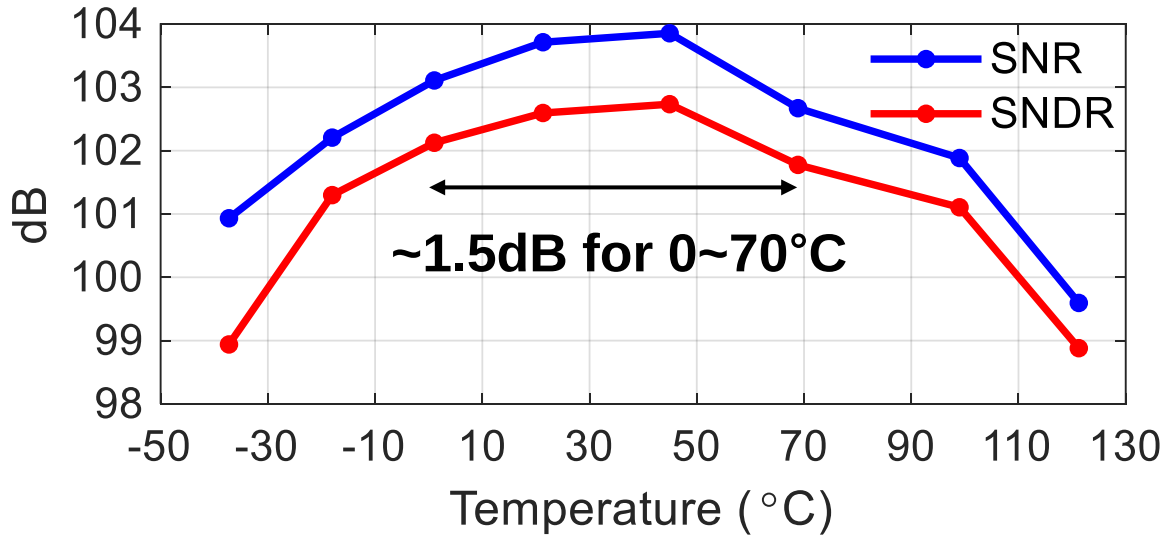




PVT Measurements







SOTA Design Comparison

	ISSCC'22 This work		VLSI'20 E. Elan	VLSI'18 B. Wang	ISSCC'21 S. Mondal	ISSCC'22 J. Steensgaard	ISSCC'20 J. Liu
Architecture	**Zoom (Cnt' + CT-IDSM)**		Zoom (SAR + DT-DSM)	DT-IDSM	CT-DSM	Multi-step SAR	NS-SAR
Process (nm)	**28**		160	65	65	180	40
Area (mm^2)	**0.014**		0.27	0.134	0.39	0.78	0.061
Supply (V)	**0.9 / 1.2**		1.8	1.2	1.2	1.8 / 5	1.1
OSR	**2^{14}**	**2^{13}**	87.5	256	150	1	25
$F_{s,nyq}$ (kS/s)	**20**	**50**	40	40	48	2000	80
Power (mW)	**0.47**	**0.59**	0.44	0.55	0.14	8.5	0.067
SNDR (dB)	**102.9**	**100.1**	106.5	100.8	100.9	105.3	90.5
FOM_S (dB)	**176.2**	**176.4**	183.1	176.4	183.3	186.0	178.2

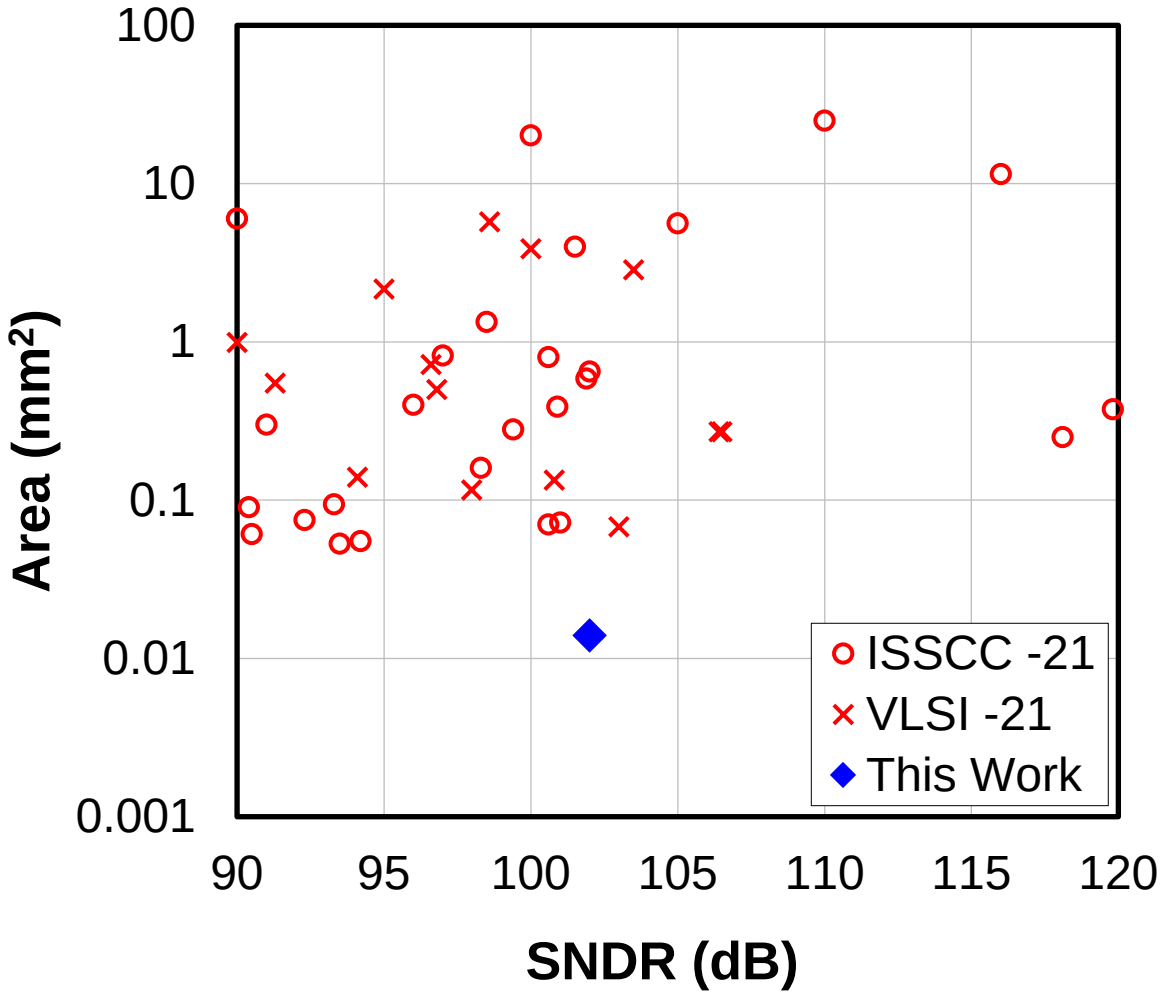
Includes decimation filter

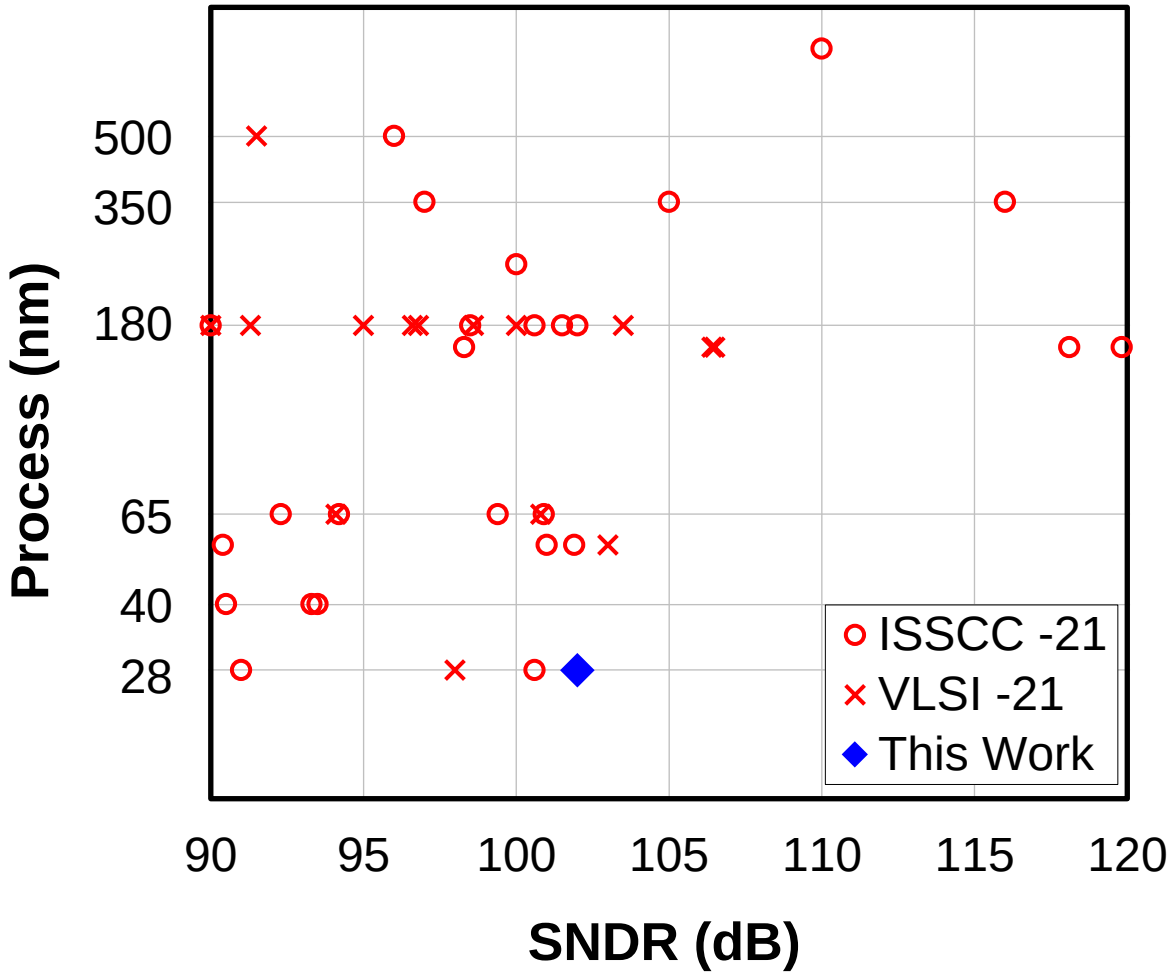
Practical Features

	ISSCC'22 This work	VLSI'20 E. Elan	VLSI'18 B. Wang	ISSCC'21 S. Mondal	ISSCC'22 J. Steensgaard	ISSCC'20 J. Liu
Architecture	**Zoom (Cnt' + CT-IDSM)**	Zoom (SAR + DT-DSM)	DT-IDSM	CT-DSM	Multi-step SAR	NS-SAR
Full-Scale CMRR @ DC	**>100dB**	>100dB	Not Support	Not Support	140dB	Not Support
Multiplexing / Single-Shot	**Incremental**	Not Support	**Incremental**	Not Support	Nyquist Sampling	Not Support
PVT	**Stable**	Stable	Stable	Not Report	Stable	Stable
Mismatch Solution	**RT-DEM**	DWA	DWA	1bit-DAC	Cal. + DEM	MES
Reference Ripple	**Code Independent**	Code Dependent	Code Dependent	Negligible (RDAC)	Code Dependent	Code Dependent
Input Network	**Cap Coupling**	Switched Cap	Switched Cap	Resistive	Switched Cap	Switched Cap

Area & Process Highlight

[B. Murmann, “ADC Survey” Jun 2021]





Conclusion

- **Prototype Highlights:**
  - Smallest for 90+dB SNDR
  - Highest SNDR for 28nm
  - Nyquist and single-end capability

- **Suggestions for designing integrated high-resolution ADC**
  - Always consider the deployment in practice
  - Take advantage of fast digital (e.g. high OSR)
  - Simple analog circuitry is preferred
  - Architecture hybridization is promising

Thanks!

Q&A