115nA@3V, ULPMark-CP score 1205 SCVR-less Dynamic Voltage-Stacking Scheme for IoT MCU

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Outline

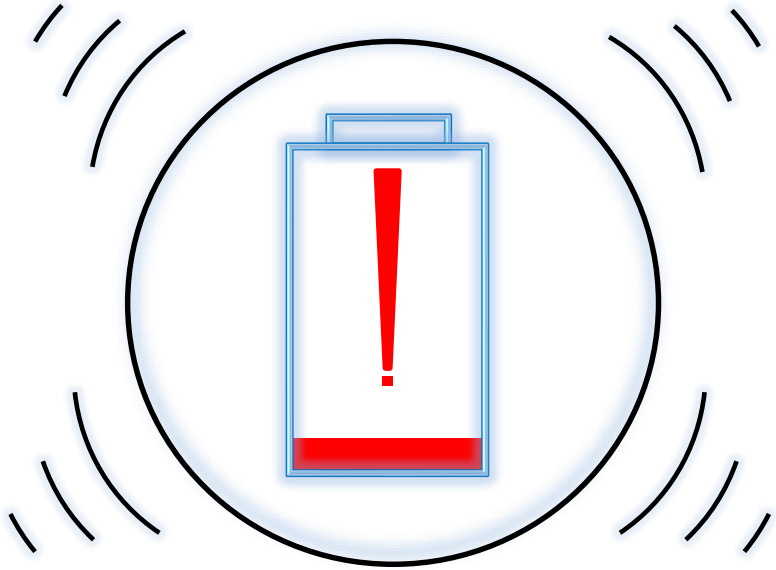
- Motivation
- Dynamic voltage-stacking scheme
  - Architecture
  - Dynamic switching scheme
  - Protection circuits
- Measurements
- Conclusions

Applications for This Work

- **Demand:** MCU is increasing demand as the core component of IoTs
- **Challenge:** Limited by battery capacity, **Ultra Low Power**

1 day: 280Wh

1 year: 5000mAh



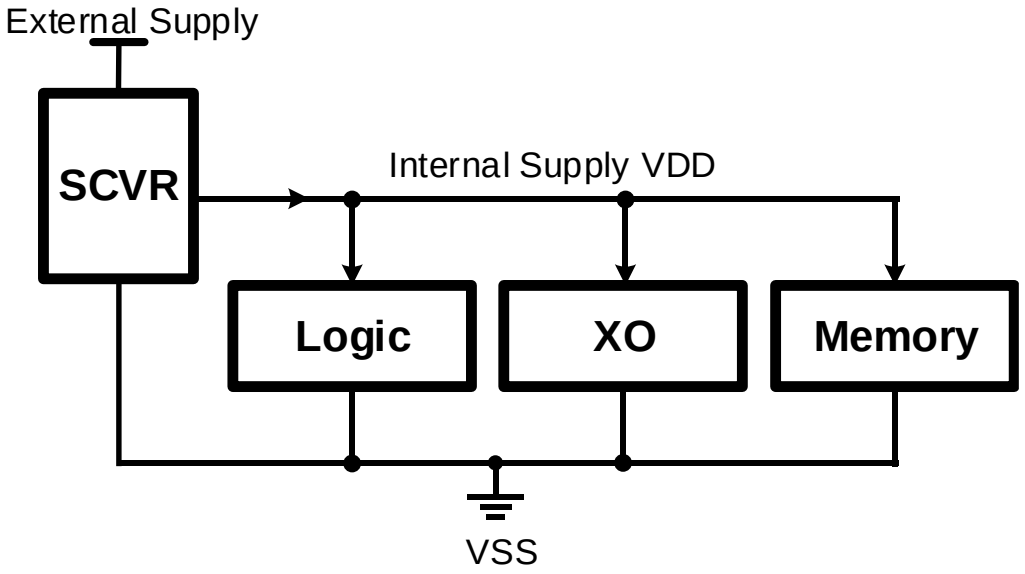
1 week: 125mAh

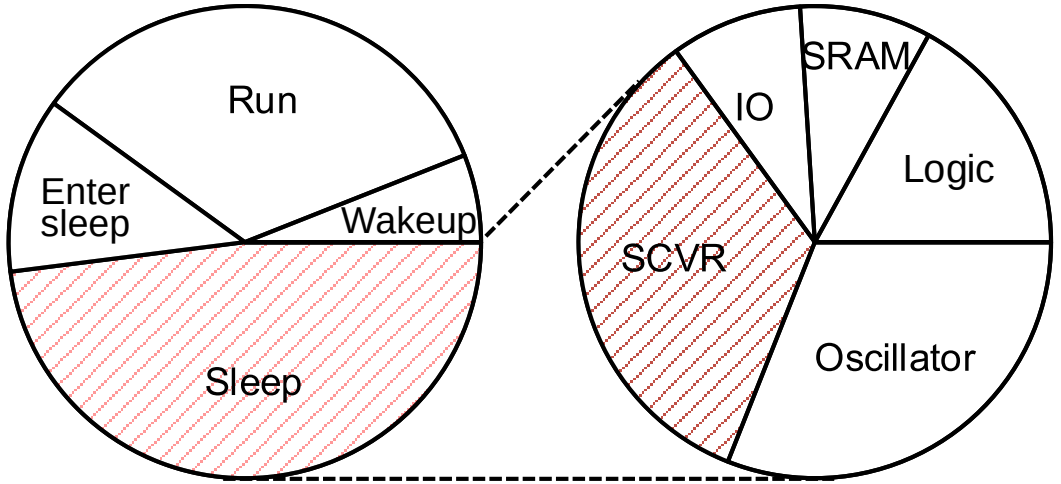
1 month: 2200mAh

Limitation of Conventional Designs

- Conventional flat architecture for both normal state and sleep state
- Sleep power breakdown of MCU
  - When duty cycle is 1:1000, sleep power accounts for most of the total power
  - The SCVR consumption accounts for most of the sleep power

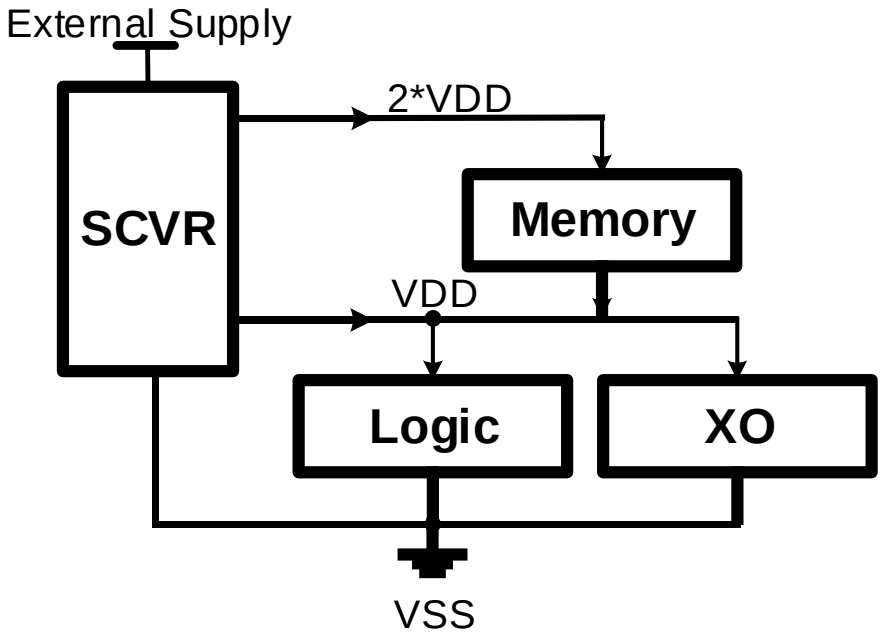
High sleep energy ☹

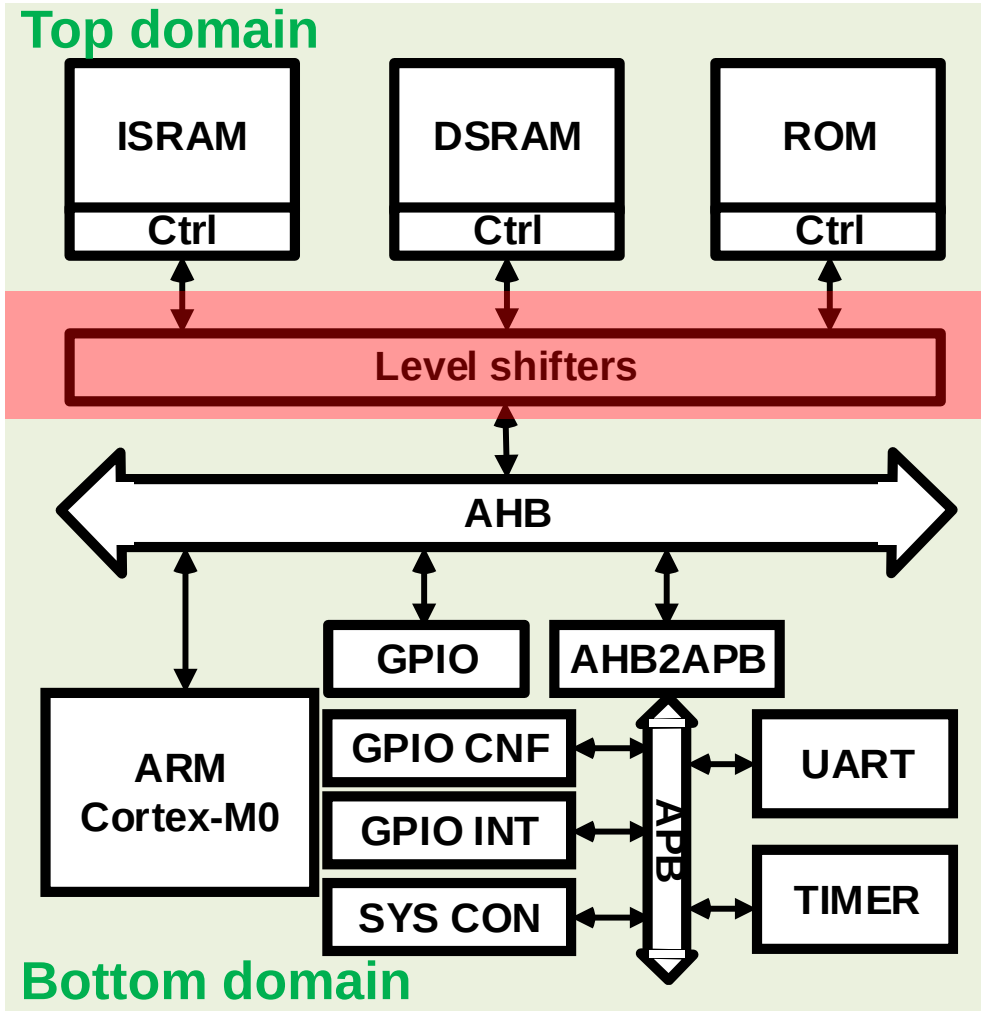




Limitation of Conventional Designs

- Prior stack architecture for normal state and sleep state*
- High dynamic power ☹
  - Too many level shifters are needed for stacked memory





*K. Blutman, et al., “A Low-Power Microcontroller in a 40-nm CMOS Using Charge Recycling”, JSSC, vlo.52, no.4, pp. 950-960, Apr. 2017.

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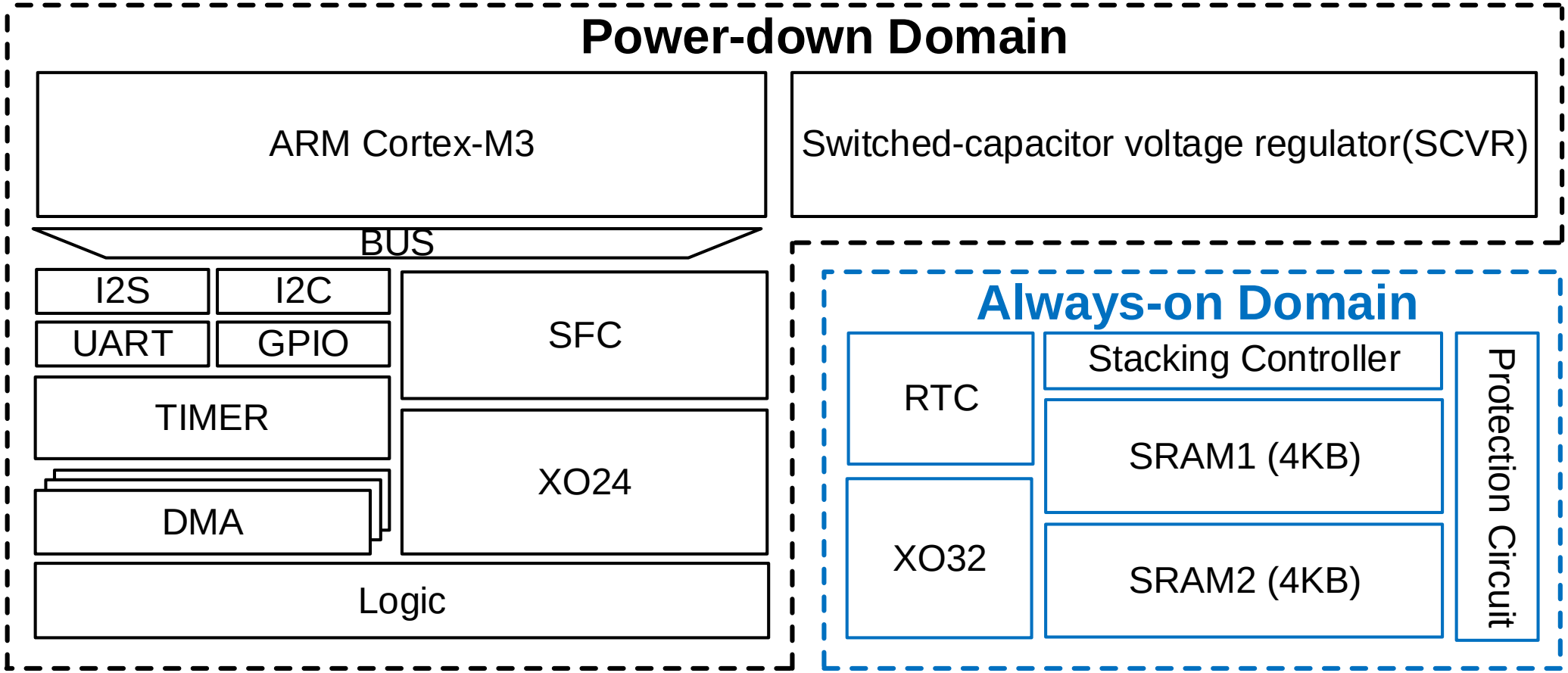
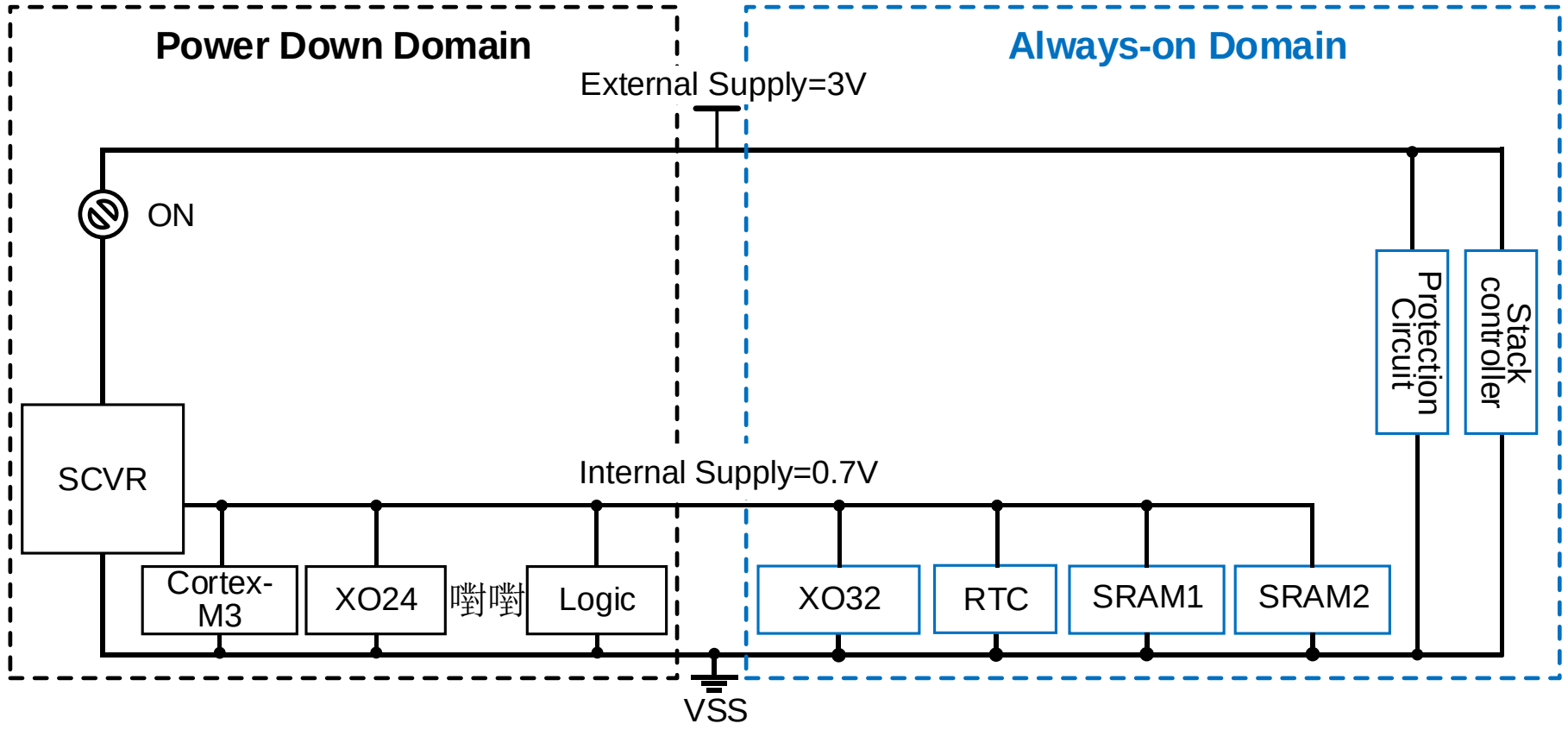
Architecture

- Modules in **power-down domain** are turned off in sleep state
- Modules in **always-on domain** need to be powered all the time



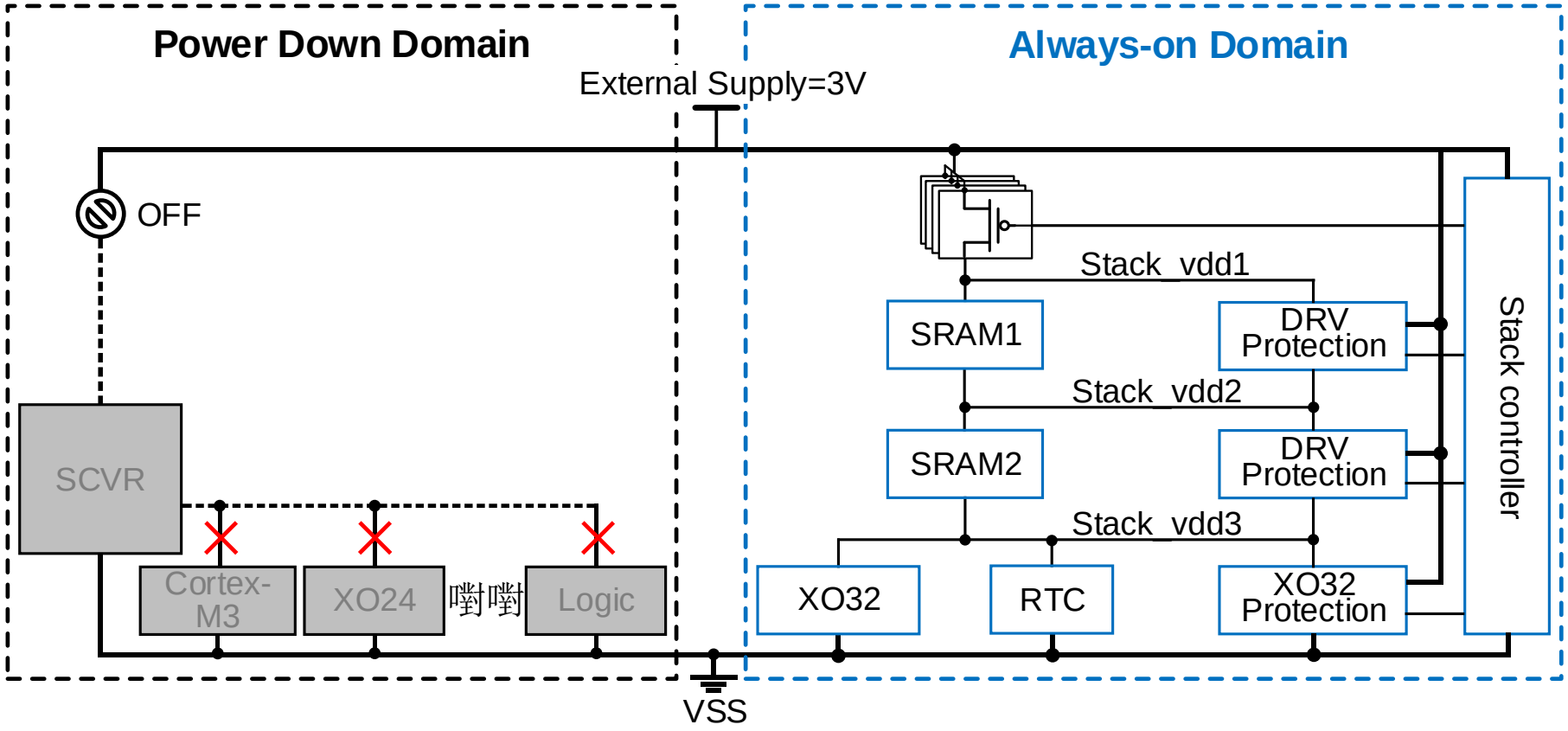
Architecture: Flat Mode for Normal State

- **Low active energy:** Modules work at low supply voltage
- Low sleep energy: Stacked scheme to reduce sleep energy



Architecture: Stack Mode for Sleep State

- Low active energy: Modules work at low supply voltage
- **Low sleep energy:** Stacked scheme to reduce sleep energy



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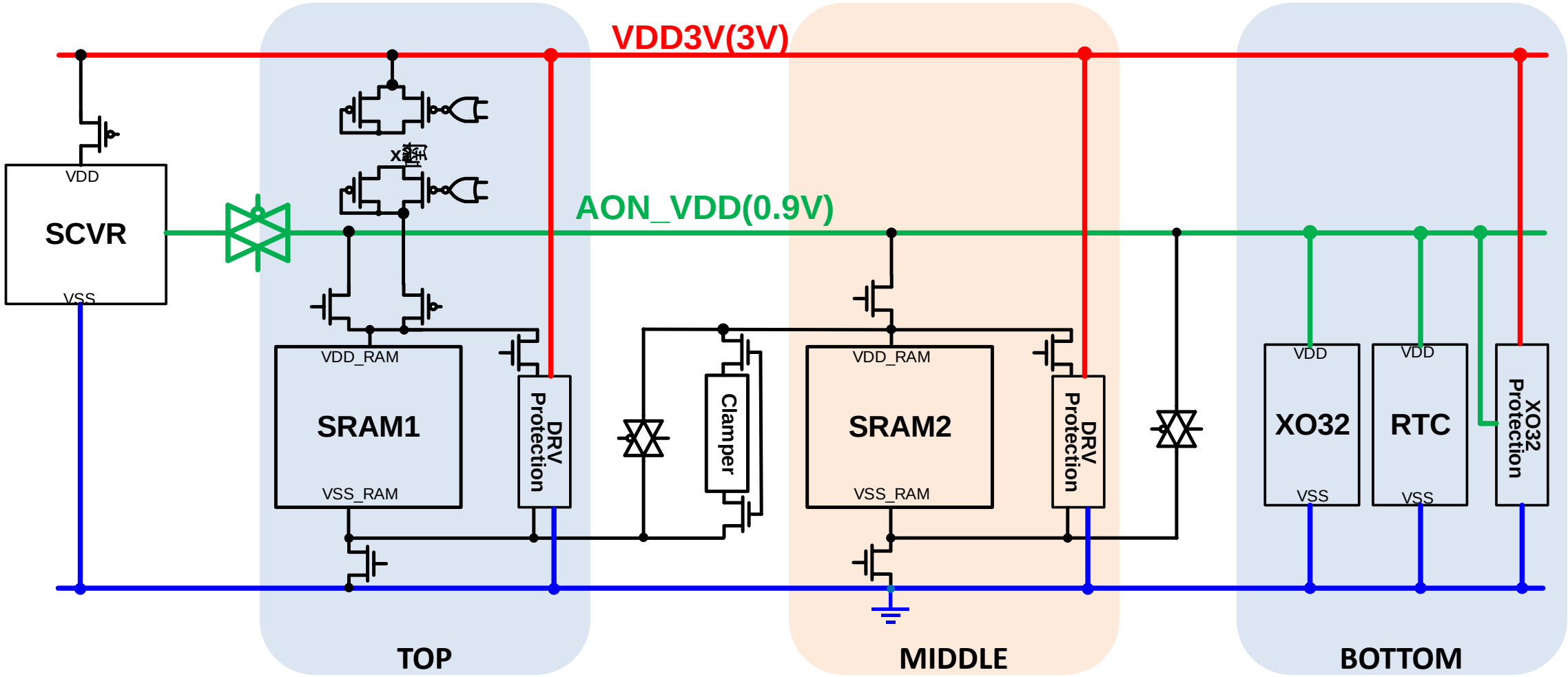
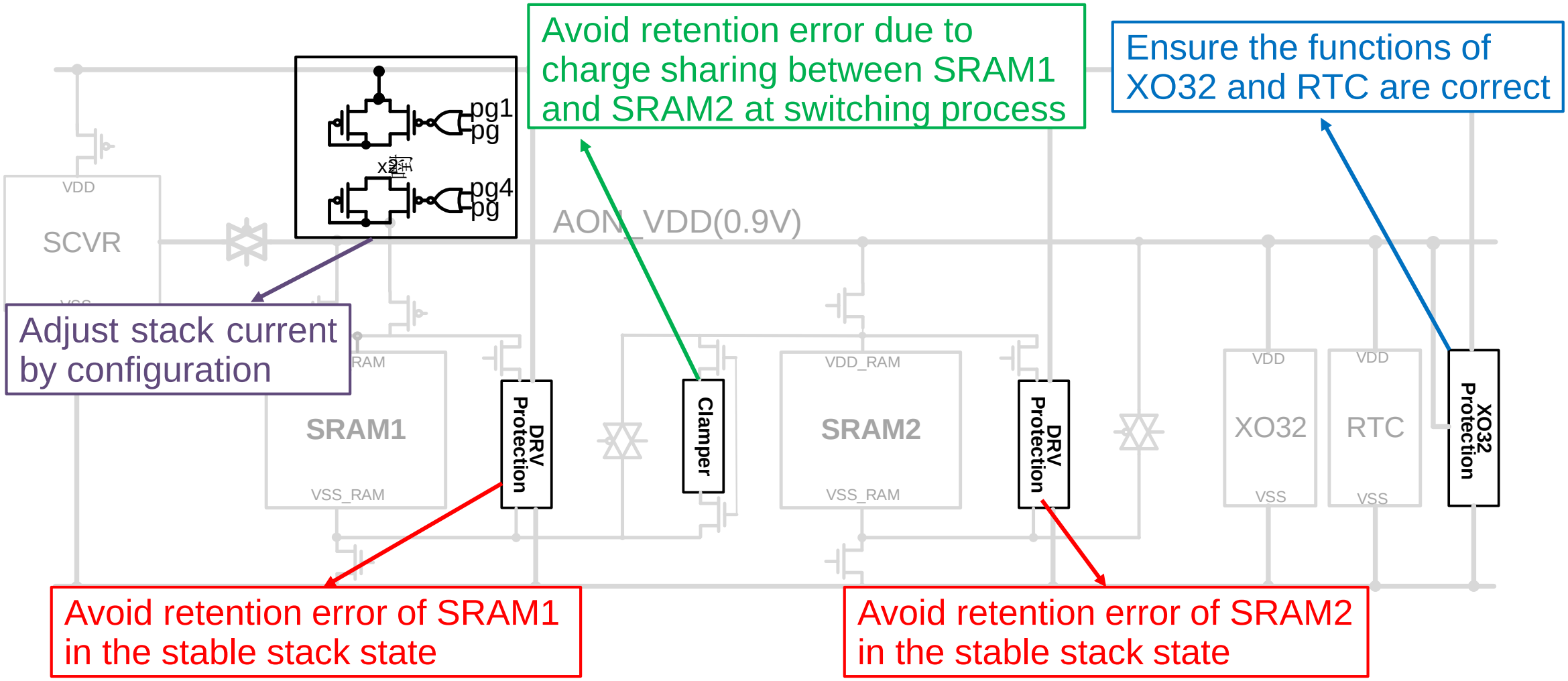
Dynamic Switching Scheme

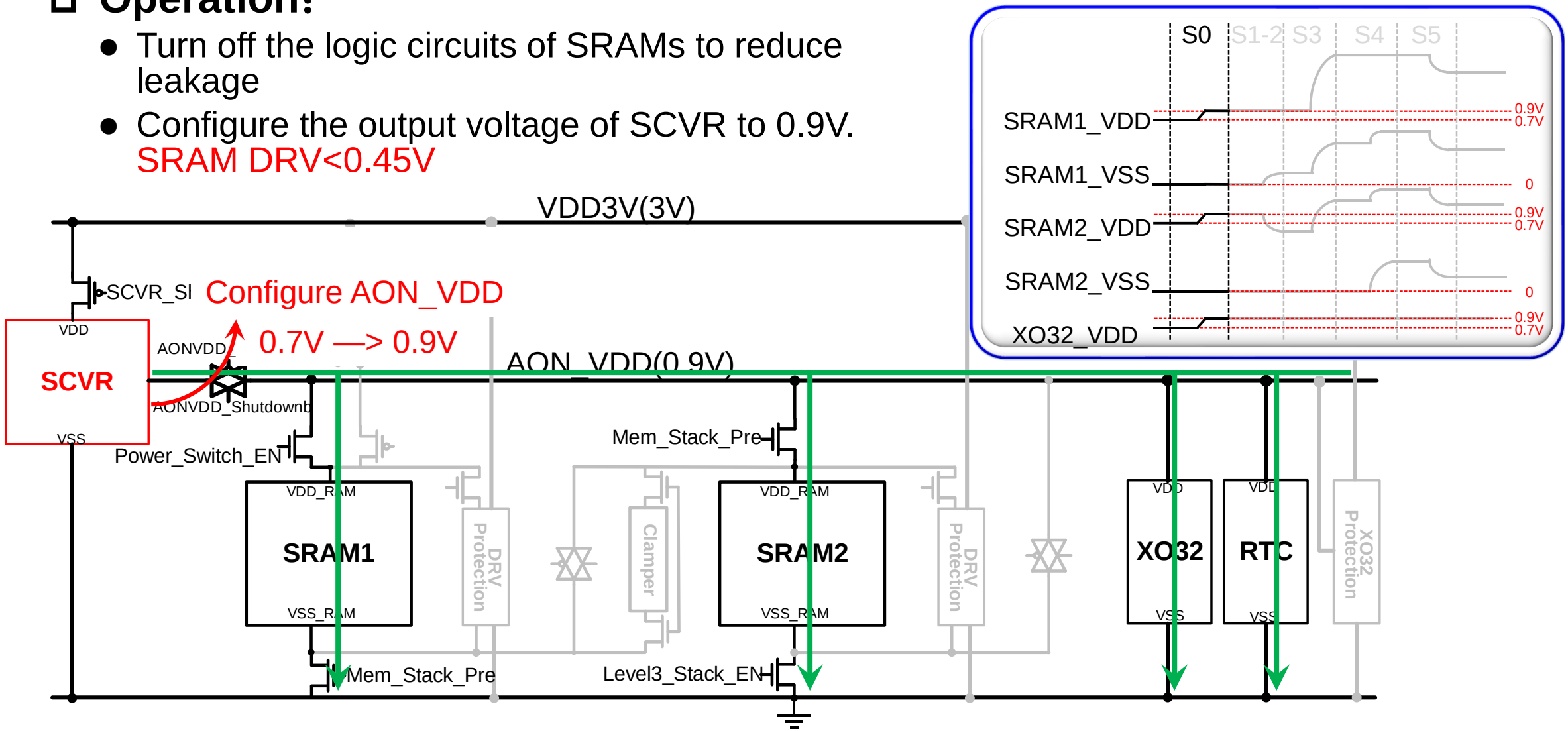


Dynamic Switching Scheme



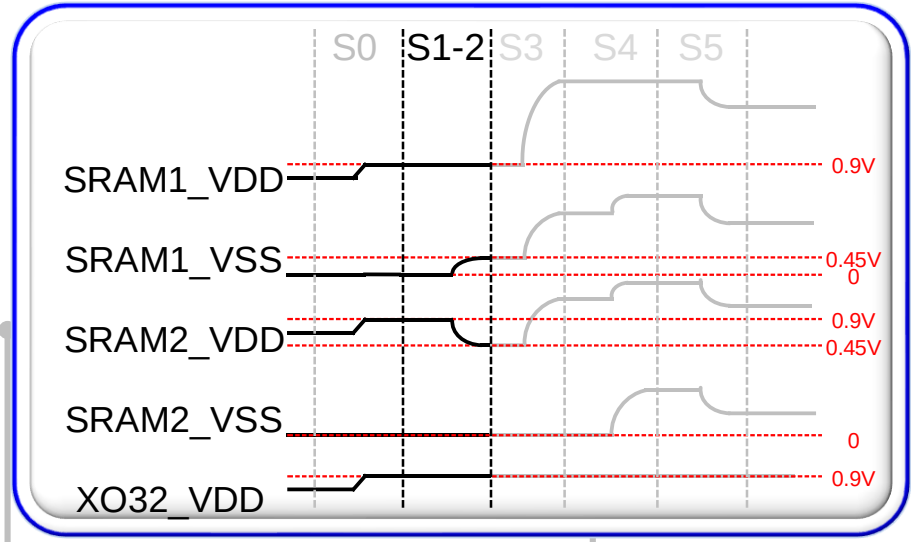
Dynamic Switching Process: Preparation

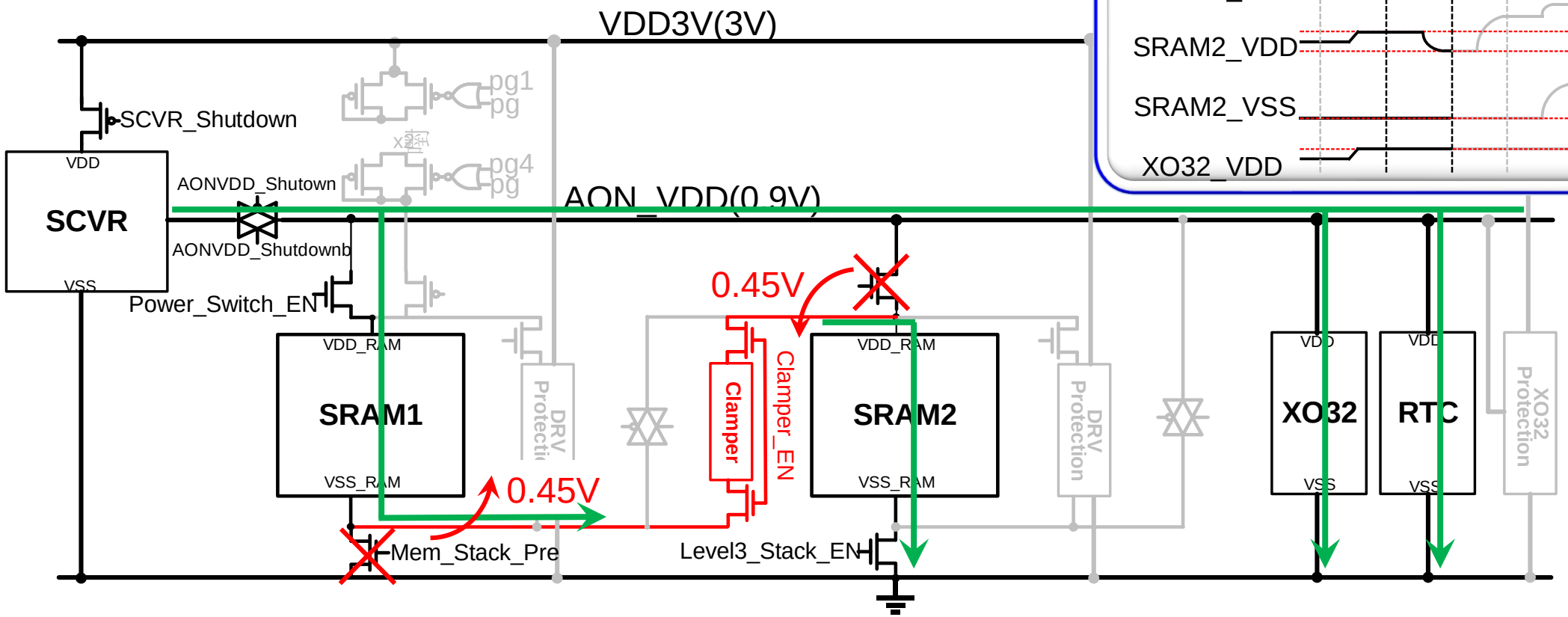
- **Operation：**
  - Turn off the logic circuits of SRAMs to reduce leakage
  - Configure the output voltage of SCVR to 0.9V. SRAM DRV<0.45V



Dynamic Switching Process: Step1

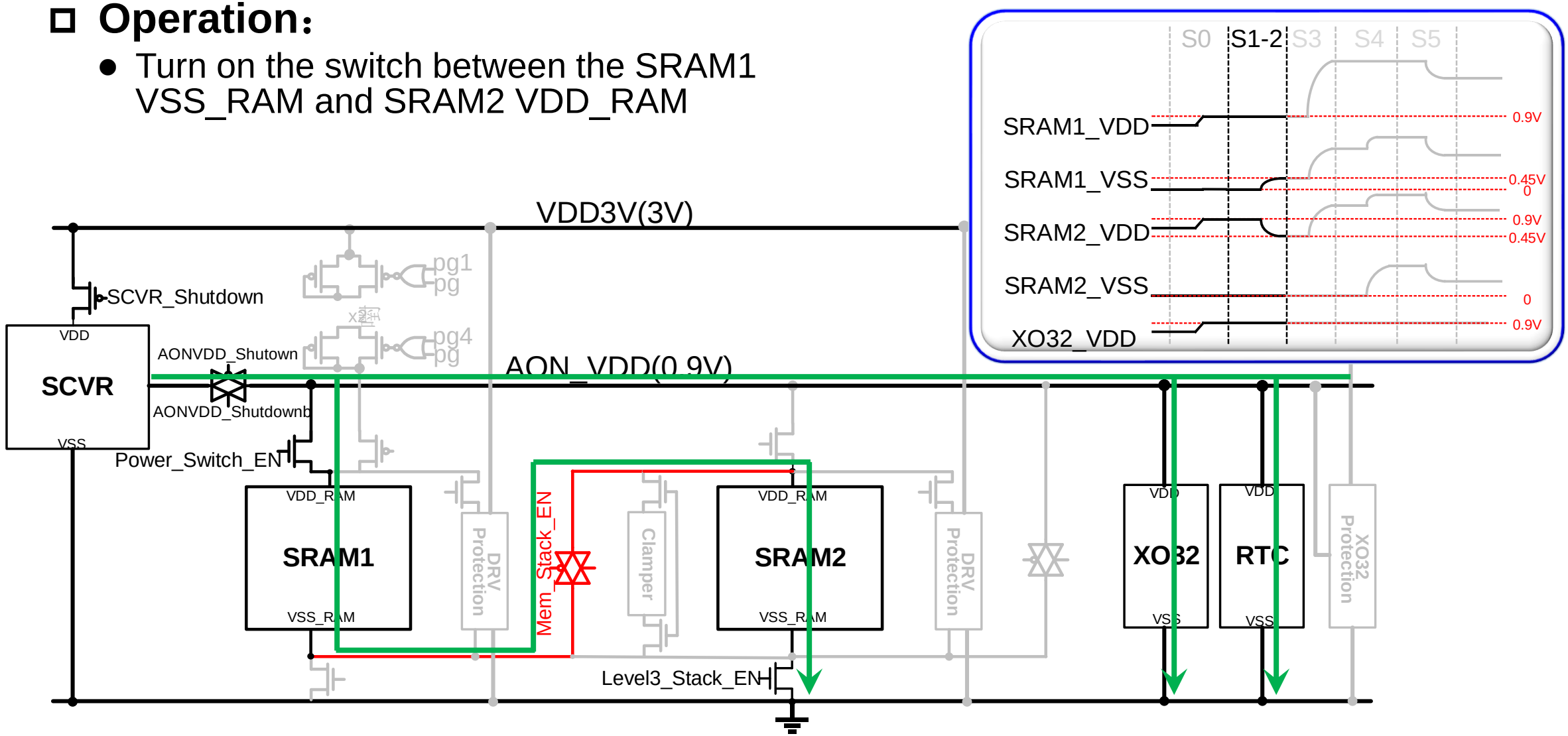
- **Operation:**
  - Turn off the switches between SRAM1 VSS_RAM and ground, SRAM2 VDD_RAM and AON_VDD
  - Turn on the clamper





Dynamic Switching Process: Step2

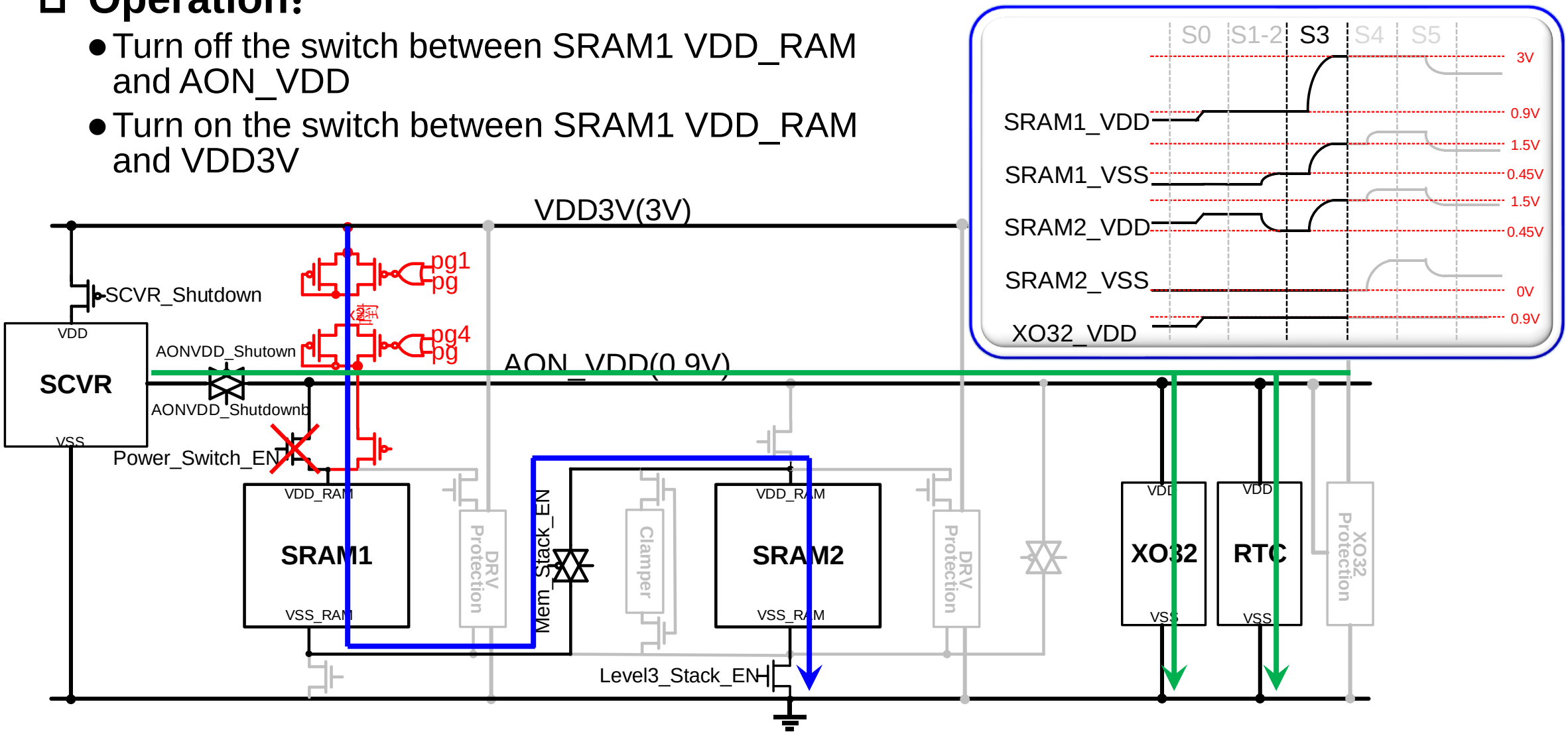
- **Operation：**
  - Turn on the switch between the SRAM1 VSS_RAM and SRAM2 VDD_RAM



Dynamic Switching Process: Step3

Operation：

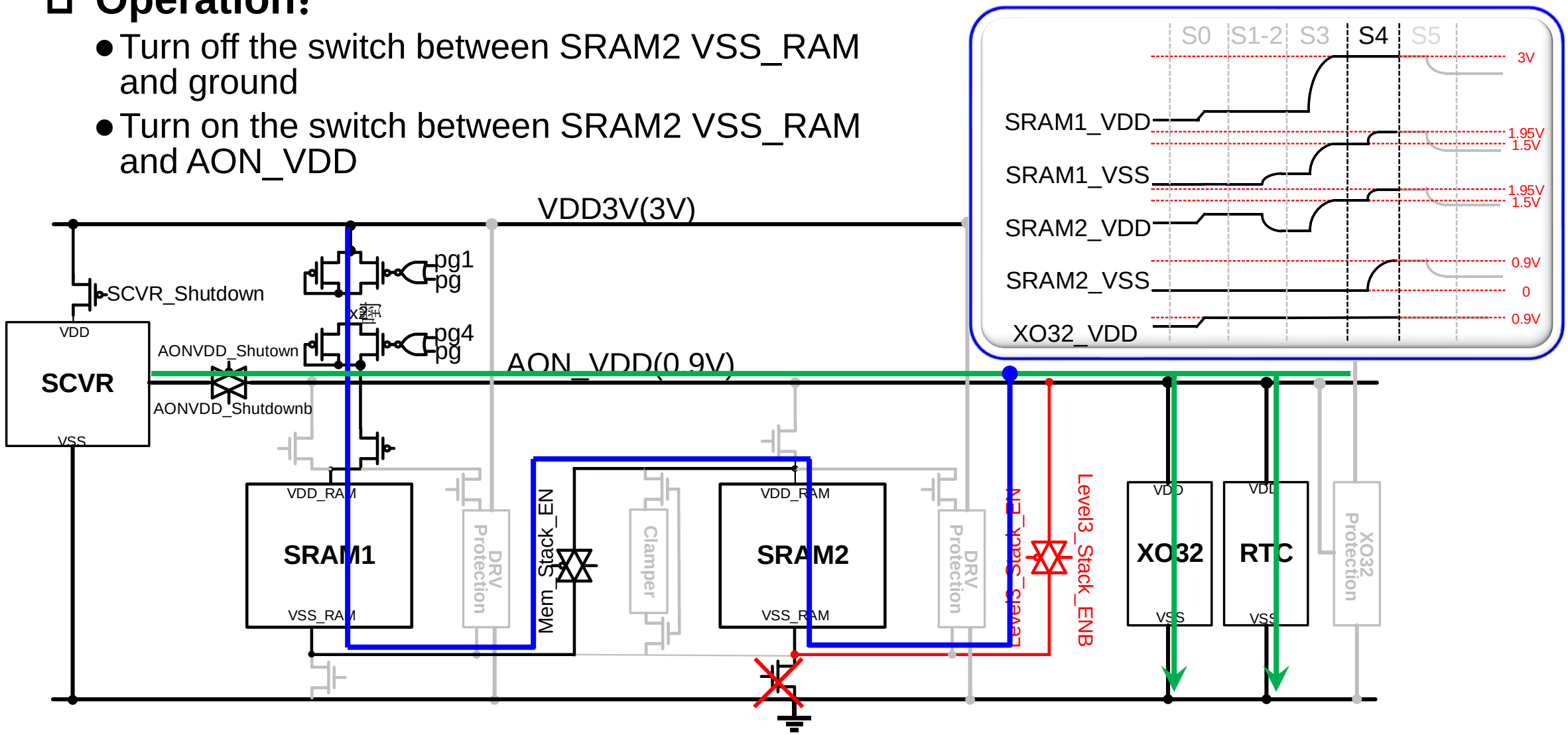
- Turn off the switch between SRAM1 VDD_RAM and AON_VDD
- Turn on the switch between SRAM1 VDD_RAM and VDD3V



Dynamic Switching Process: Step4

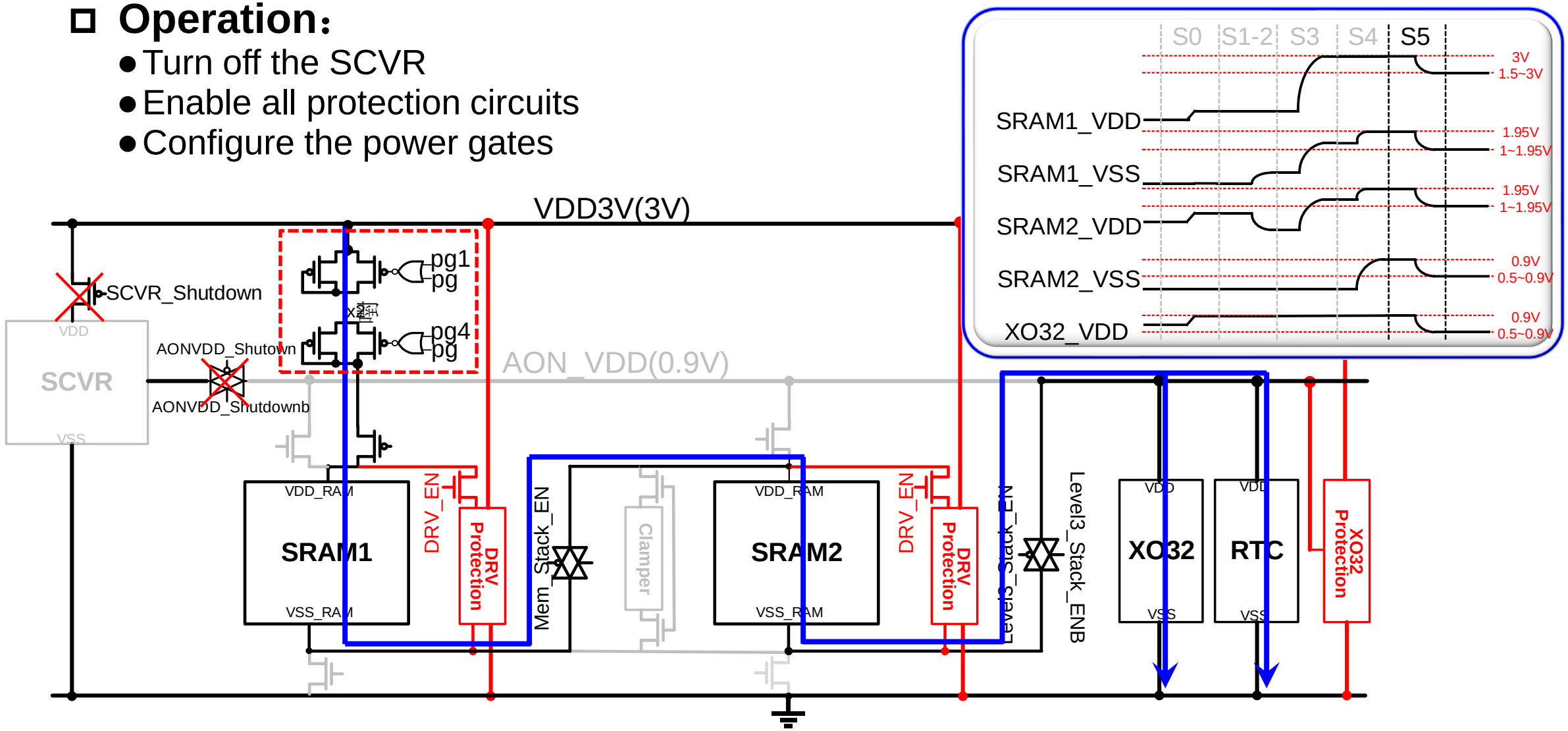
Operation:

- Turn off the switch between SRAM2 VSS_RAM and ground
- Turn on the switch between SRAM2 VSS_RAM and AON_VDD



Dynamic Switching Process: Step5

- **Operation：**
  - Turn off the SCVR
  - Enable all protection circuits
  - Configure the power gates



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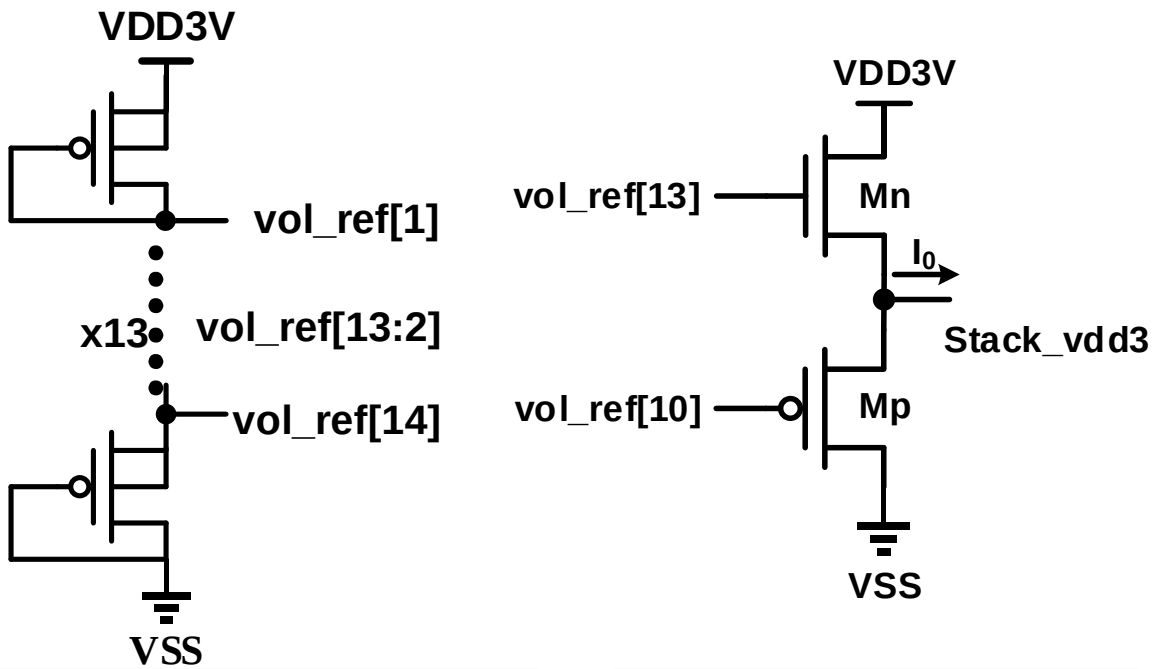
Protection Circuits: XO32 Protection Circuits

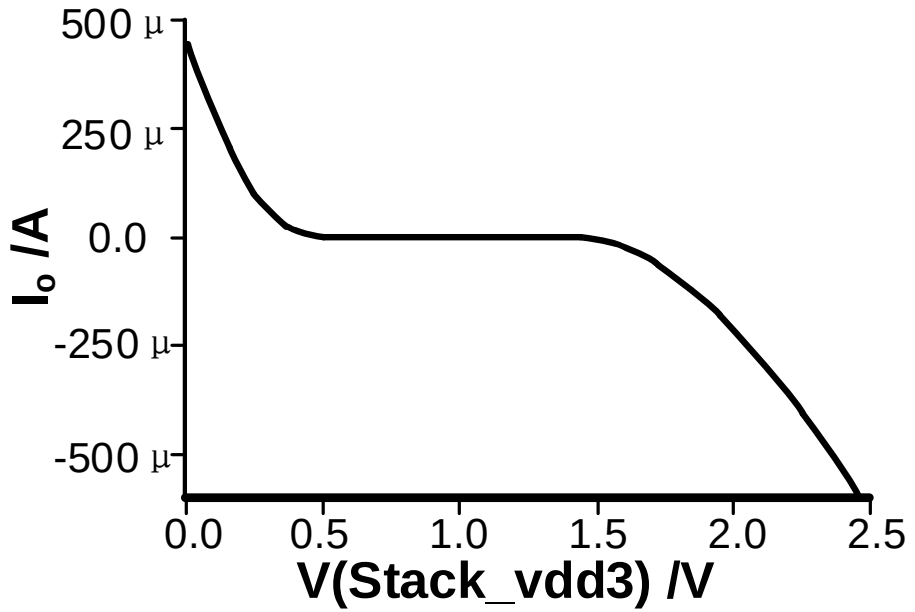
- **Purpose:** Avoid the supply voltage of XO32 and RTC >1.5V, or <0.5V

Scheme



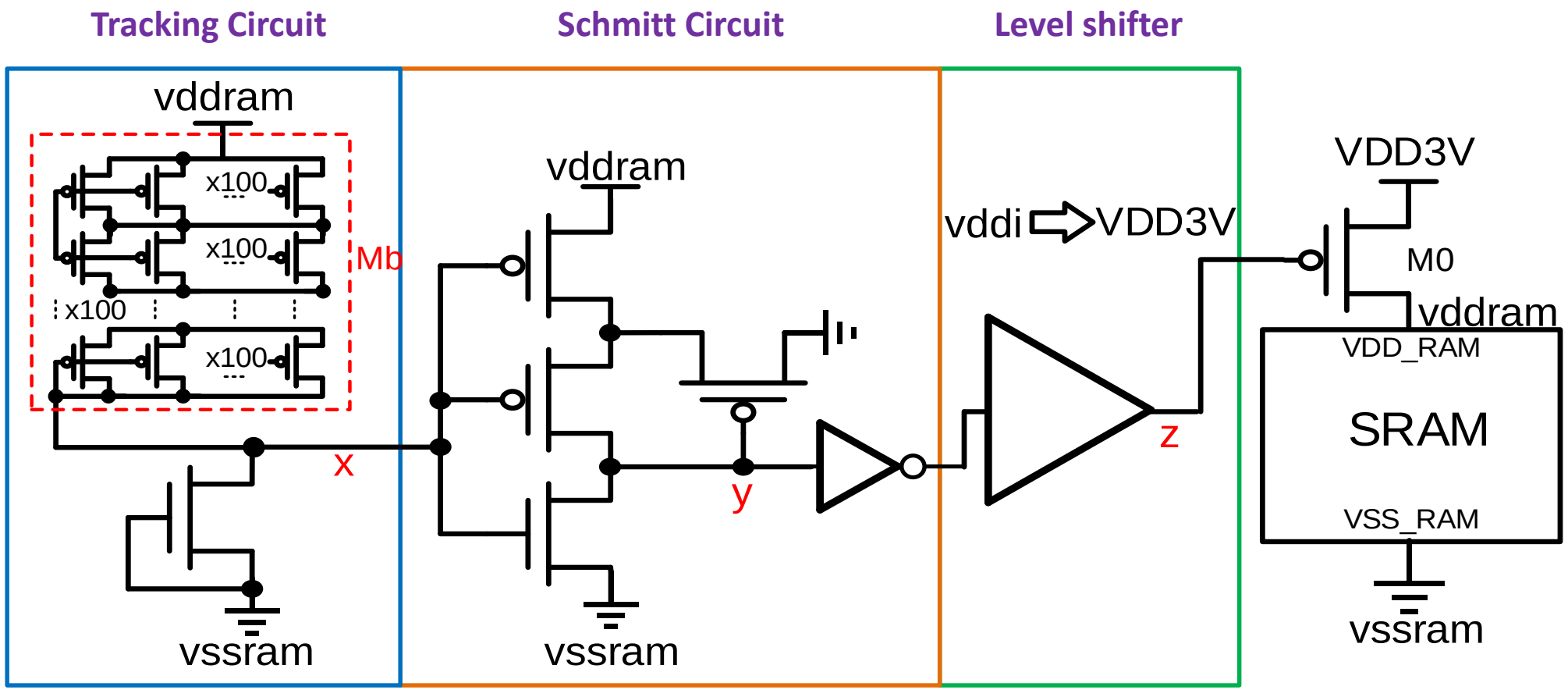
- Generate reference voltages to adjust the protection circuit
- Use Mn & Mp to charge or discharge Stack_vdd3

Simulation waveform



- When Stack_vdd3<0.5V, it will be charged
- When Stack_vdd3>1.5V, it'll be discharged

Protection Circuits: DRV Protection Circuits



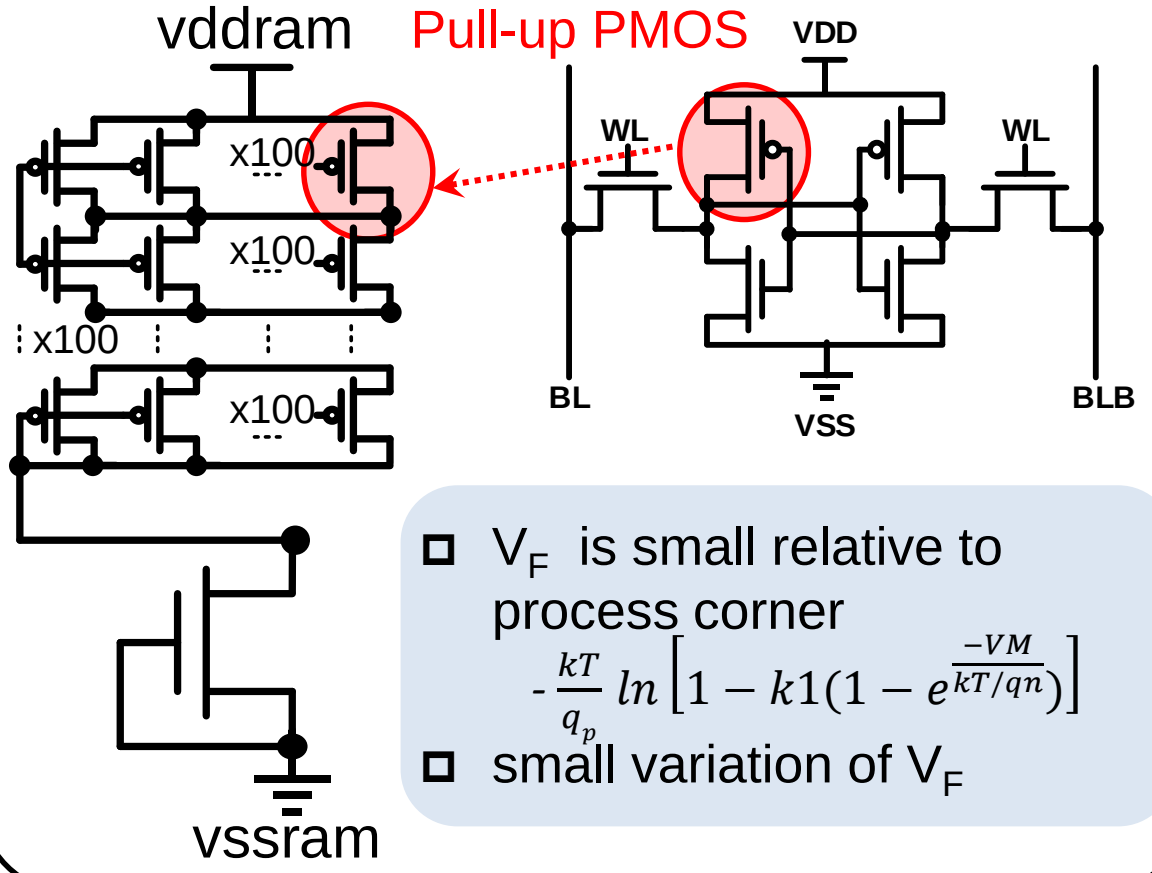
$$V_{vddram}\text{-}V_{vssram} = V_M + V_F > V_{DRV}$$

$$\approx V_M - \frac{kT}{q_p} ln\left[1 - k1\left(1 - e^{\frac{-VM}{kT/qn}}\right)\right]$$

- V_F: Forward voltage of Mb
- V_M: Switch voltage of Schmitt circuit

Track Circuit: Process Variation Tracking

V_F *vs.* Process Variation

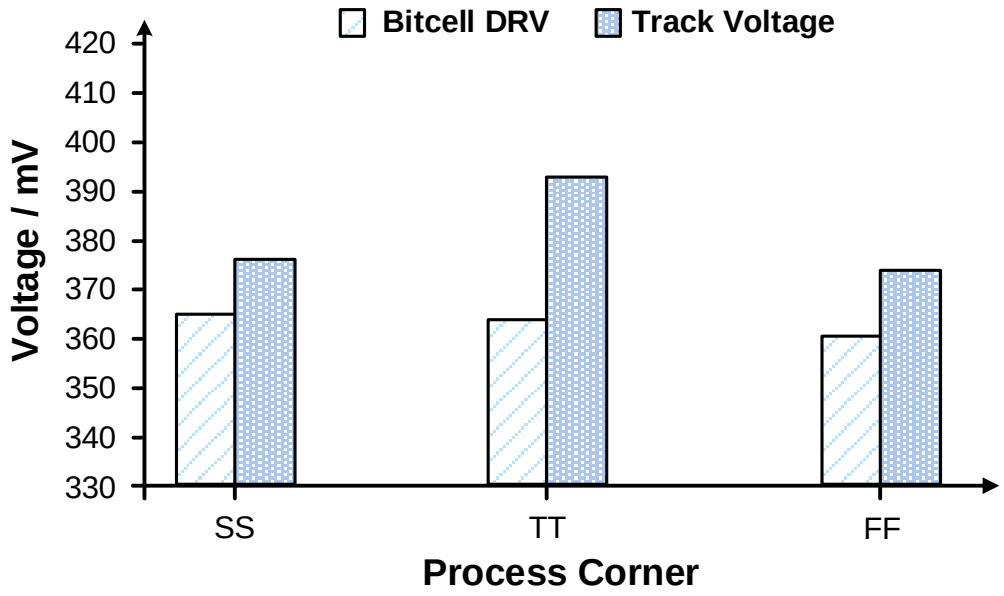


- V_F is small relative to process corner

$$-\frac{kT}{q_p} ln\left[1 - k1\left(1 - e^{\frac{-VM}{kT/qn}}\right)\right]$$

- small variation of V_F

V_{DRV} *vs.* Process Variation

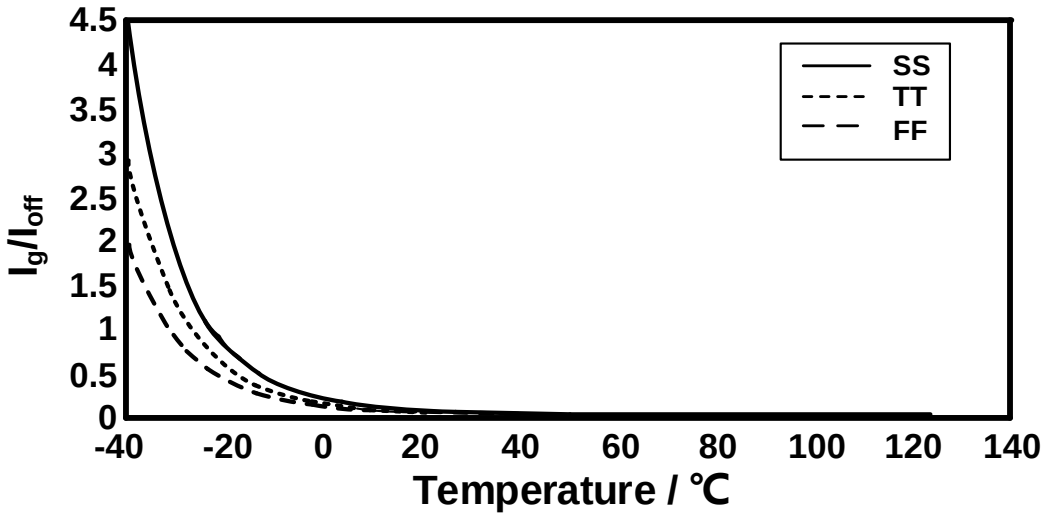


- V_{DRV} small relative to process corner

Track Circuit: Temperature Tracking

DRV: Negative Temperature Coefficient

I_{off}: subthreshold leakage I_g: gate leakage



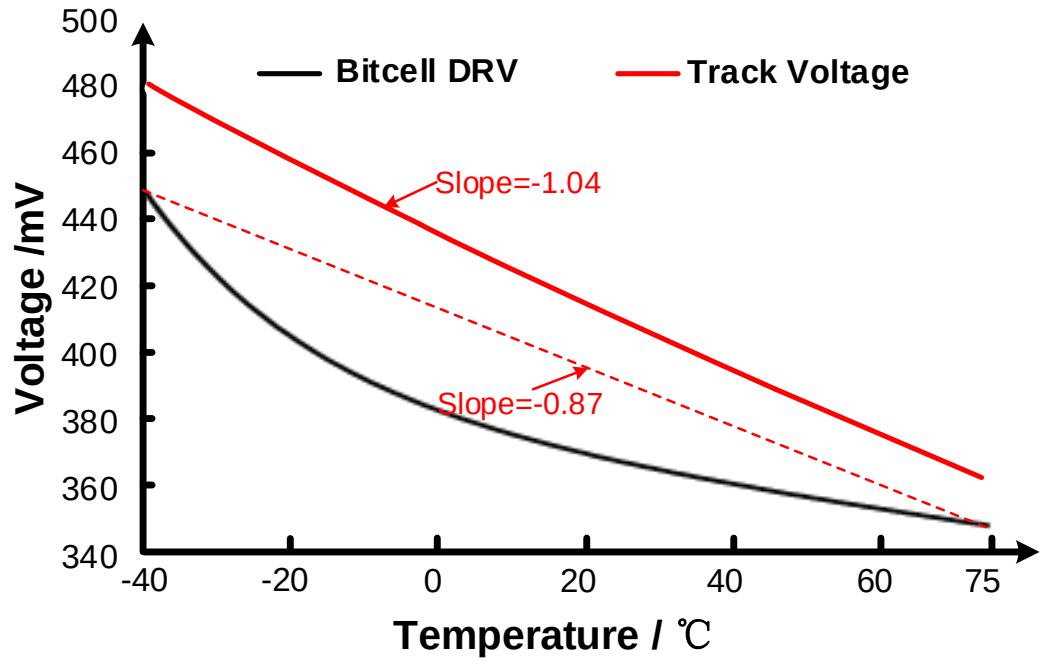
Temp↑ → I_g/I_{off}↓ → Stability Yield*↑ → Min DRV↓

Track Voltage: Negative Temperature Coefficient

$$V_{vddram} - Vvs_{sram} \approx V_M - \frac{kT}{q_p} \ln\left[1 - k1\left(1 - e^{\frac{-VM}{kT/qn}}\right)\right]$$

Temp↑ → T↑ → Track voltage↓

Traceability of Track Voltage to DRV



- DRV and track voltage are both negative temperature coefficient
- The coefficients are similar

* R. Kanj et al., "Gate Leakage Effects on Yield and Design Considerations of PD/SOI SRAM Designs", Int. Symp. Quality Electronic Design, pp. 33-40, Mar. 2007.

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- **Measurements**
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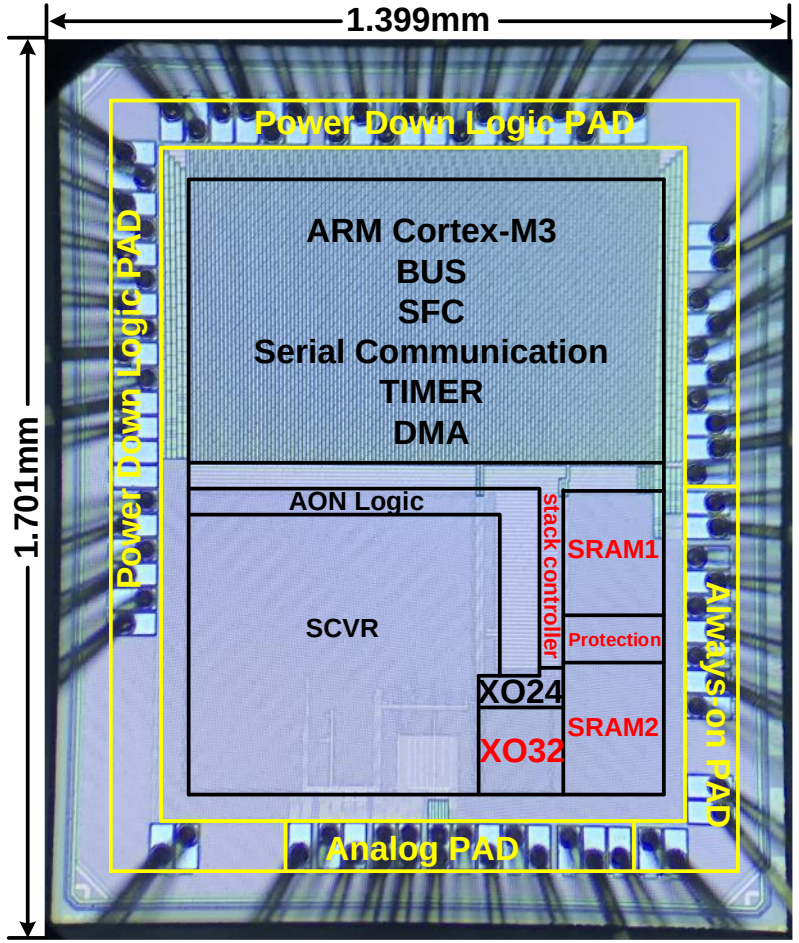
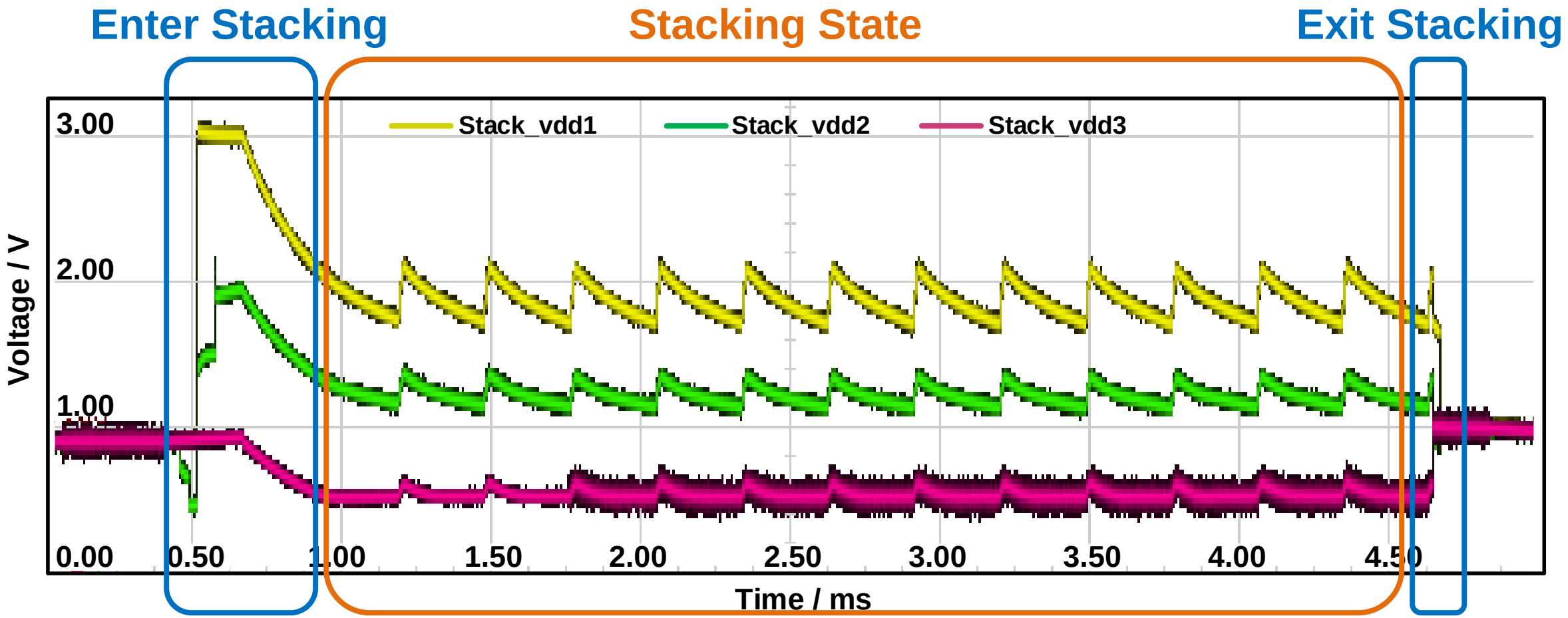
Stack MCU Chip



Technology	TSMC40nm ULP
Area	2.38mm^2
Supply voltage	0.7V@Active
	3V@Sleep
Frequency	24MHz@Active
	32KHz@Sleep
RAM Size	8K Bytes
Sleep Current	115nA
ULPMark-CP Score	1205

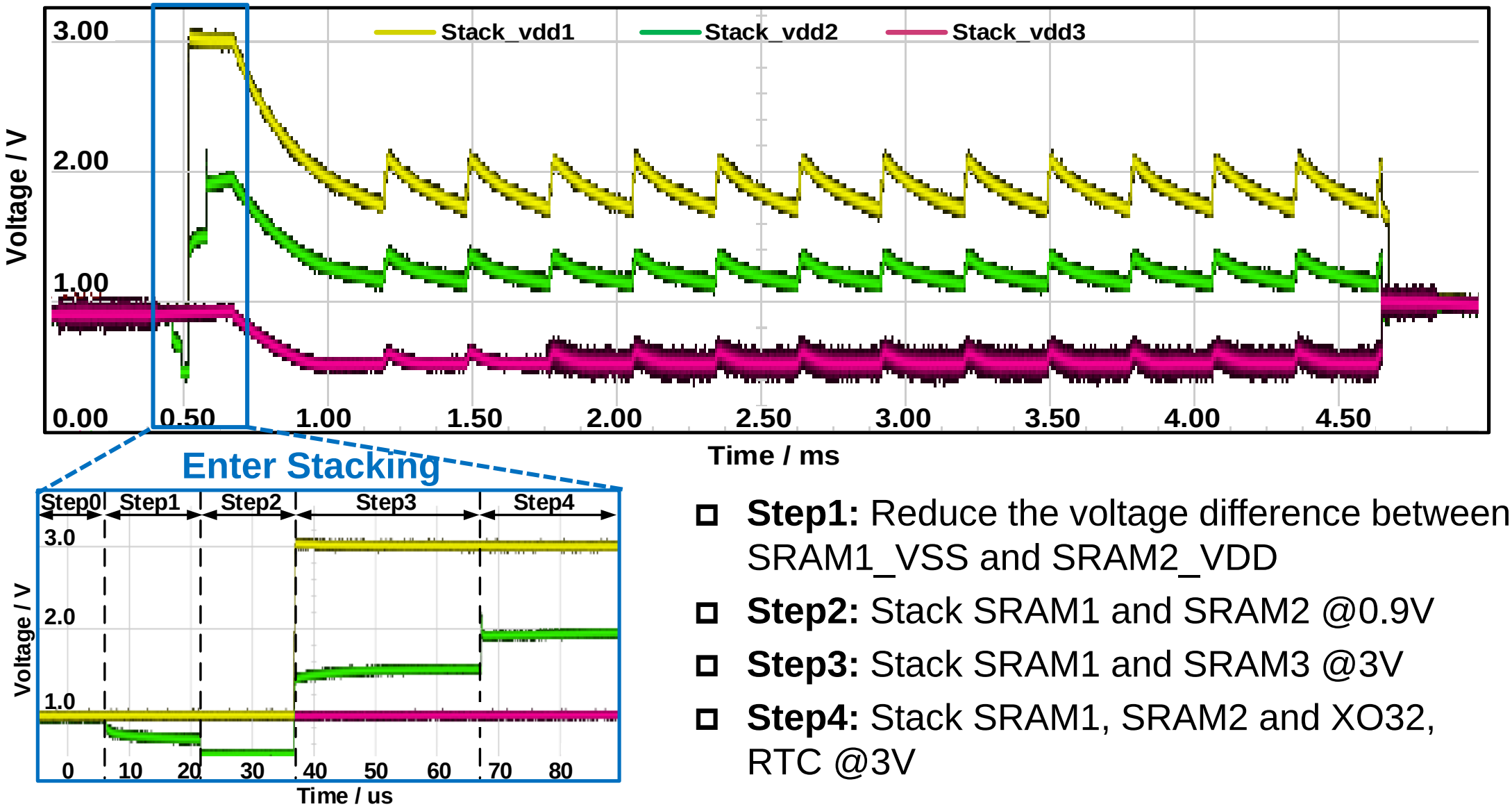
- **Architecture 1:** flat with SCVR in normal operation and sleep state
- **Architecture 2:** dynamic flat/stack architecture in which the flat mode is in normal operation and the stack mode is in sleep without SCVR

Measured Stacking Voltage



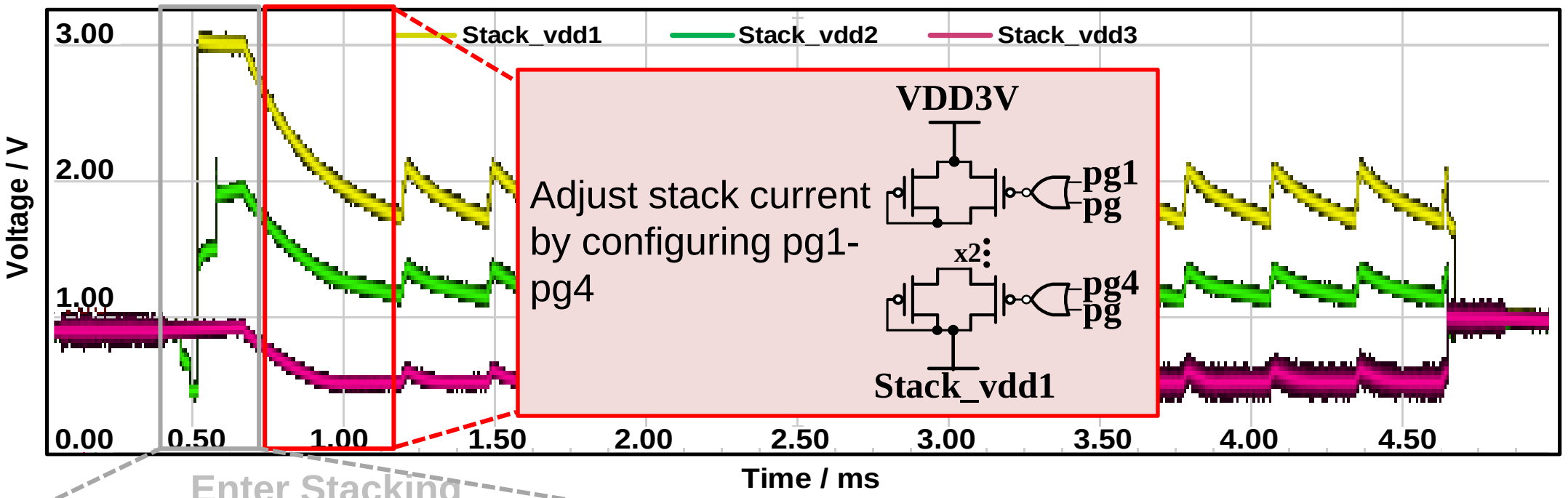
Stack_vdd1: SRAM1 VDD_RAM ╱ Stack_vdd2: SRAM2 VDD_RAM ╱ Stack_vdd3: X032 & RTC VDD

Measured Stacking Voltage

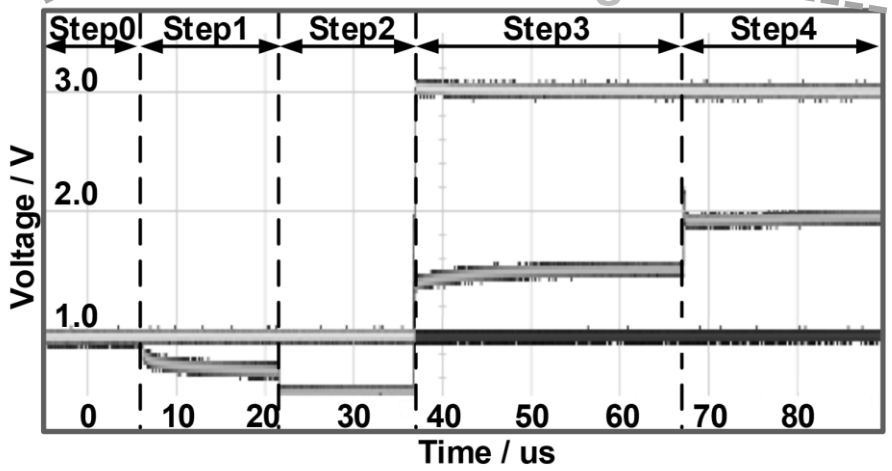


- **Step1:** Reduce the voltage difference between SRAM1_VSS and SRAM2_VDD
- **Step2:** Stack SRAM1 and SRAM2 @0.9V
- **Step3:** Stack SRAM1 and SRAM3 @3V
- **Step4:** Stack SRAM1, SRAM2 and XO32, RTC @3V

Measured Stacking Voltage



Enter Stacking



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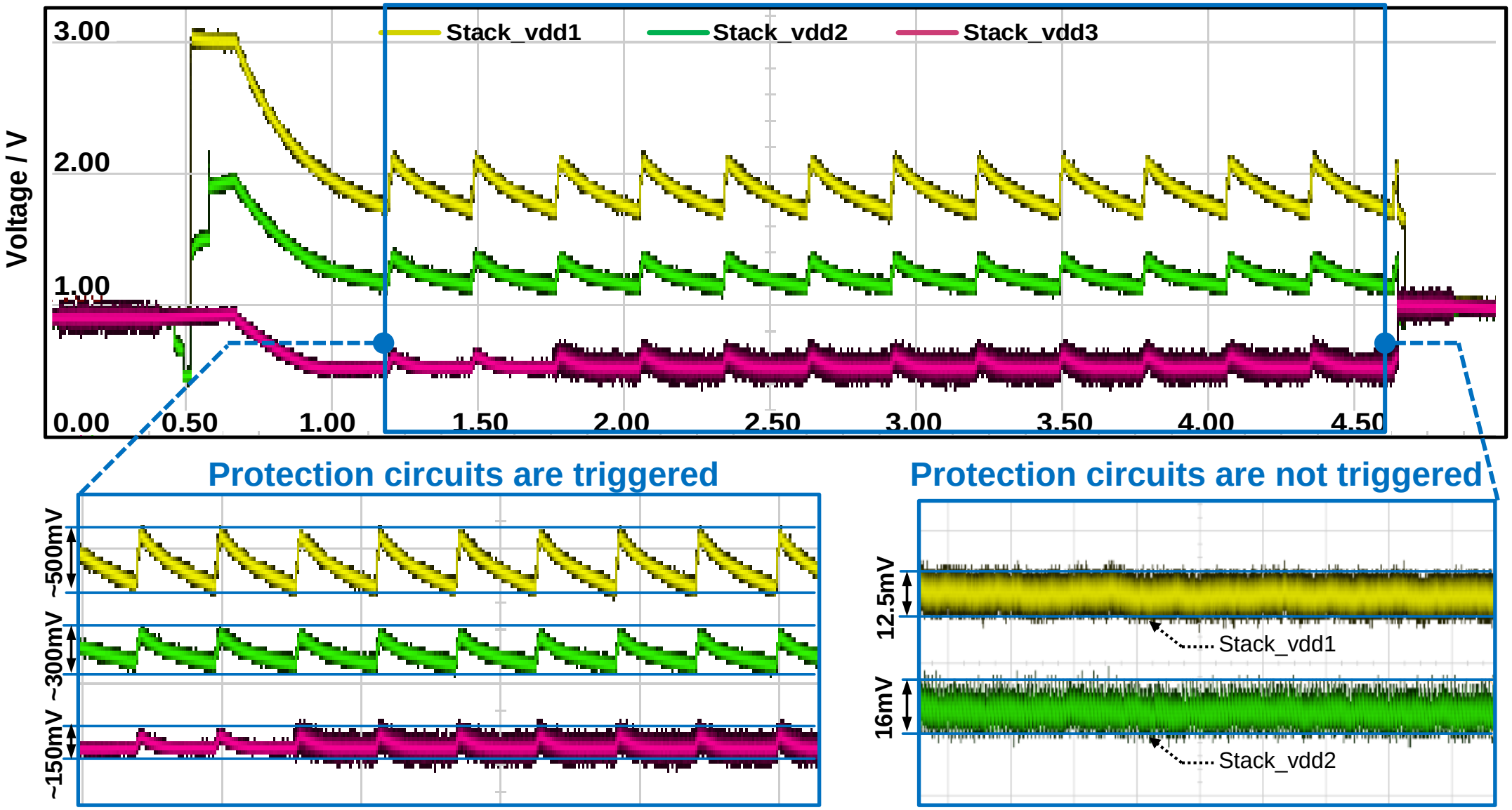
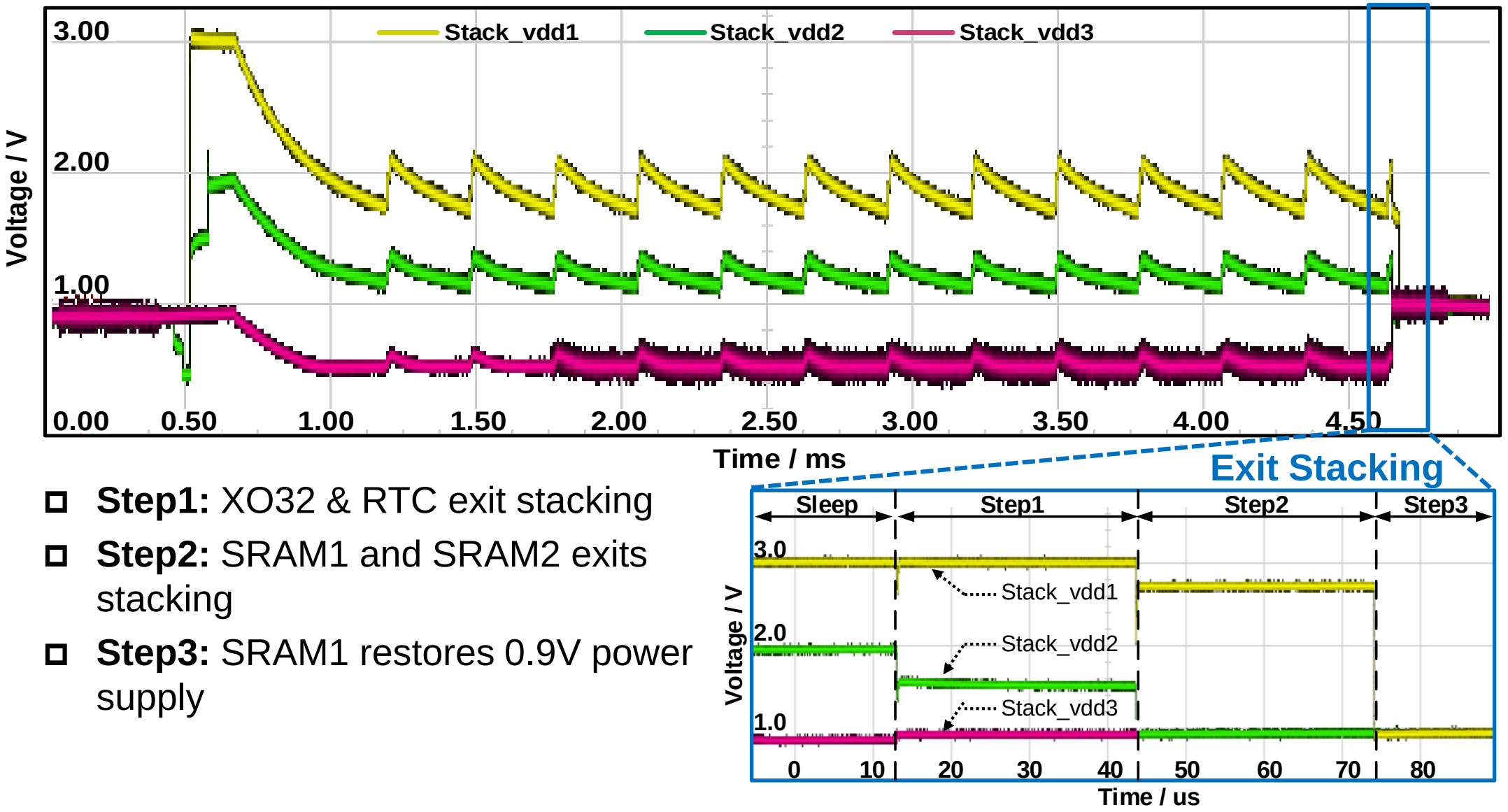
Measured Stacking Voltage

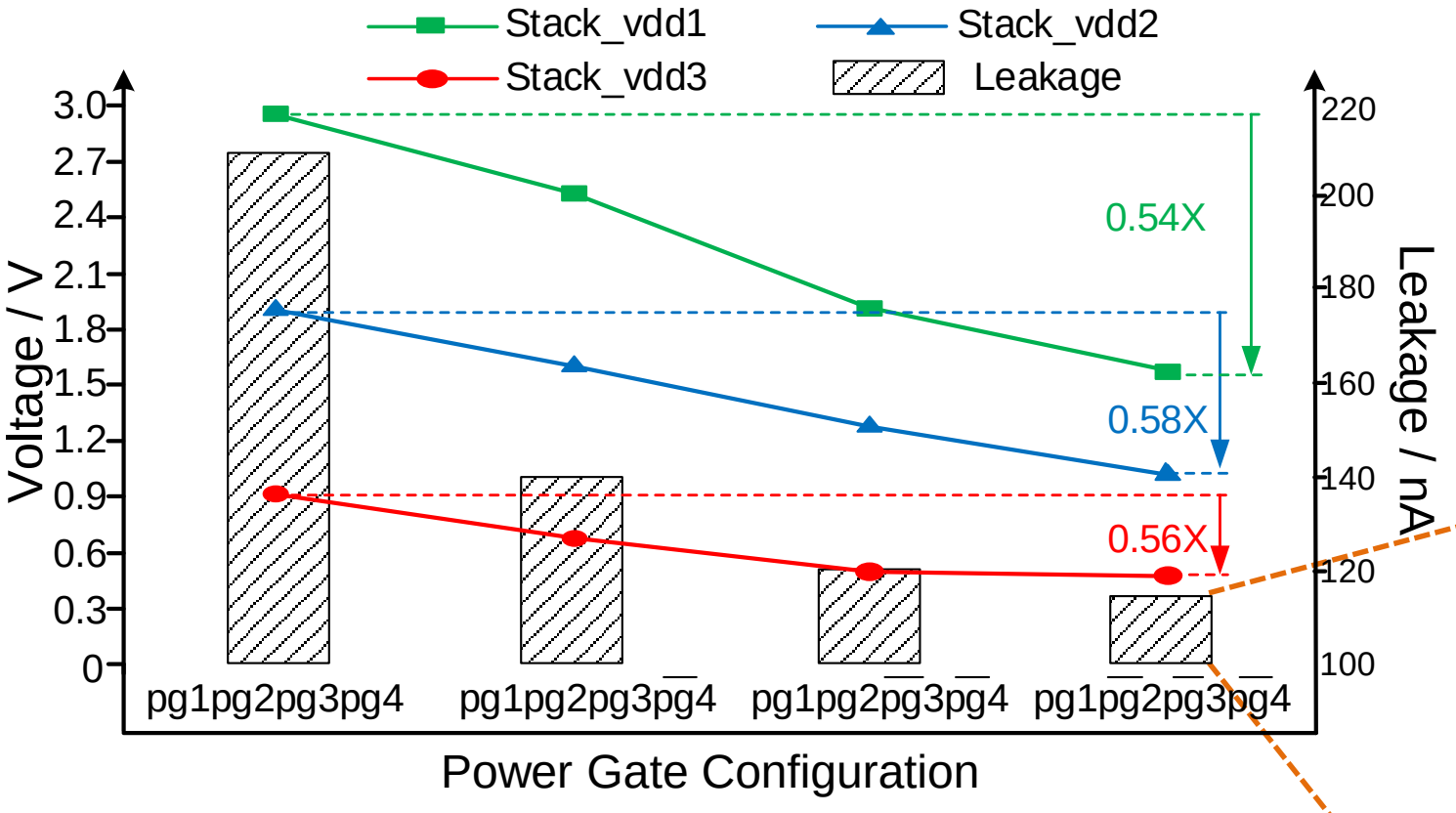


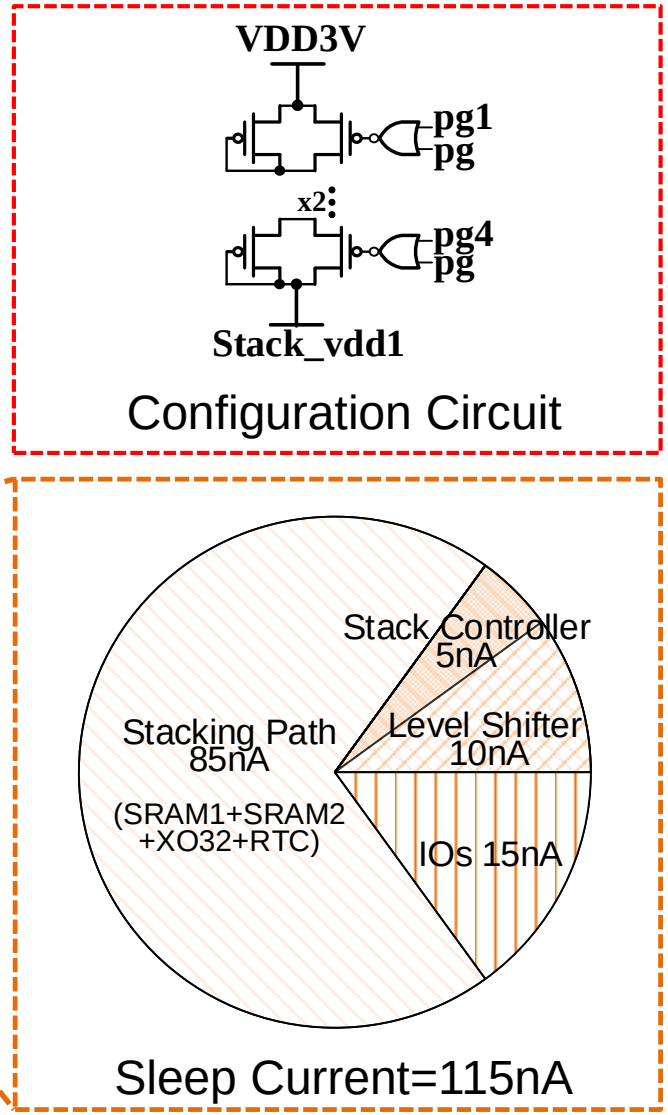
Measured Stacking Voltage



- **Step1:** XO32 & RTC exit stacking
- **Step2:** SRAM1 and SRAM2 exits stacking
- **Step3:** SRAM1 restores 0.9V power supply

Measurements at Different PG Configuration



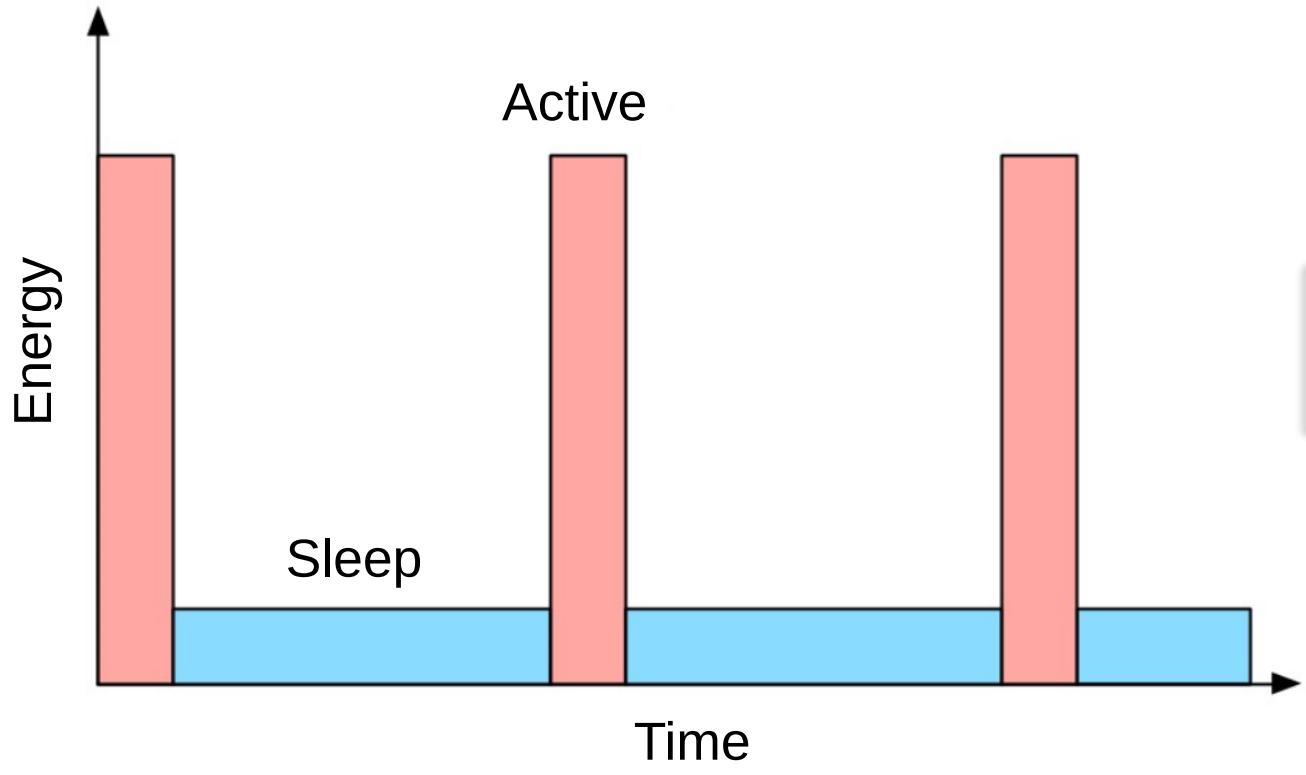


- Stack voltages are reduced by ~40% from (pg1pg2pg3pg4) to (pg1$\overline{pg2}\,\overline{pg3}\,\overline{pg4}$)
- Sleep current is as low as 115nA @pg1$\overline{pg2}\,\overline{pg3}\,\overline{pg4}$

ULPMark-CP*

ULPMark-CP: EEMBC's proposed benchmark, focusing on MCU's power and energy

ULPMark-CP Score: inverse of the average power times 1000



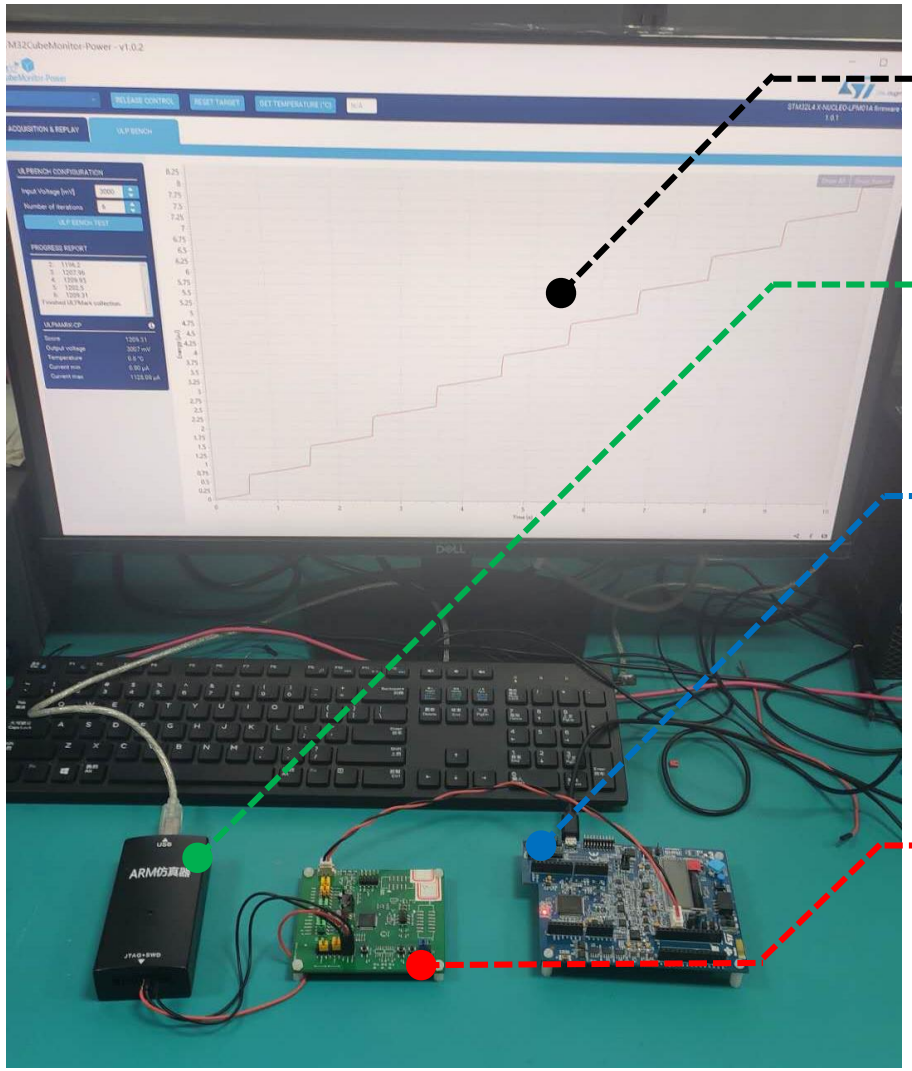
ULPMark-CP Scores

Hardware	Vendor Score	Cert.	Core Profile (3.0V)↓
ON Semiconductor RSL10 Rev 1.0	√	√	1090
Nanjing Low Power IC Technology Institute Co., Ltd LP5100 Rev.1	√	√	856**
Ambiq Micro APOLLO512-KBR Rev.A3			395
Ambiq Micro APOLLO512-KBR Rev.A3	√	√	378
Renesas Electronics R7F0E01182CFP	√	√	366

* Embedded Microprocessor Benchmark Consortium, "EEMBC ULPMark benchmark," Oct. 2014, Accessed on Nov. 23rd, 2020, < https://www.eembc.org/products/#ulp>

** Another chip of Nanjing Low Power IC Technology Institute Co., Ltd. The score is certified.

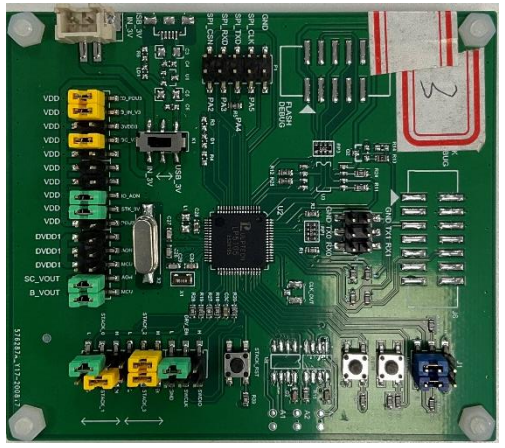
ULPMark-CP Measurement Setup



PC
Control the measurement setup and view the results

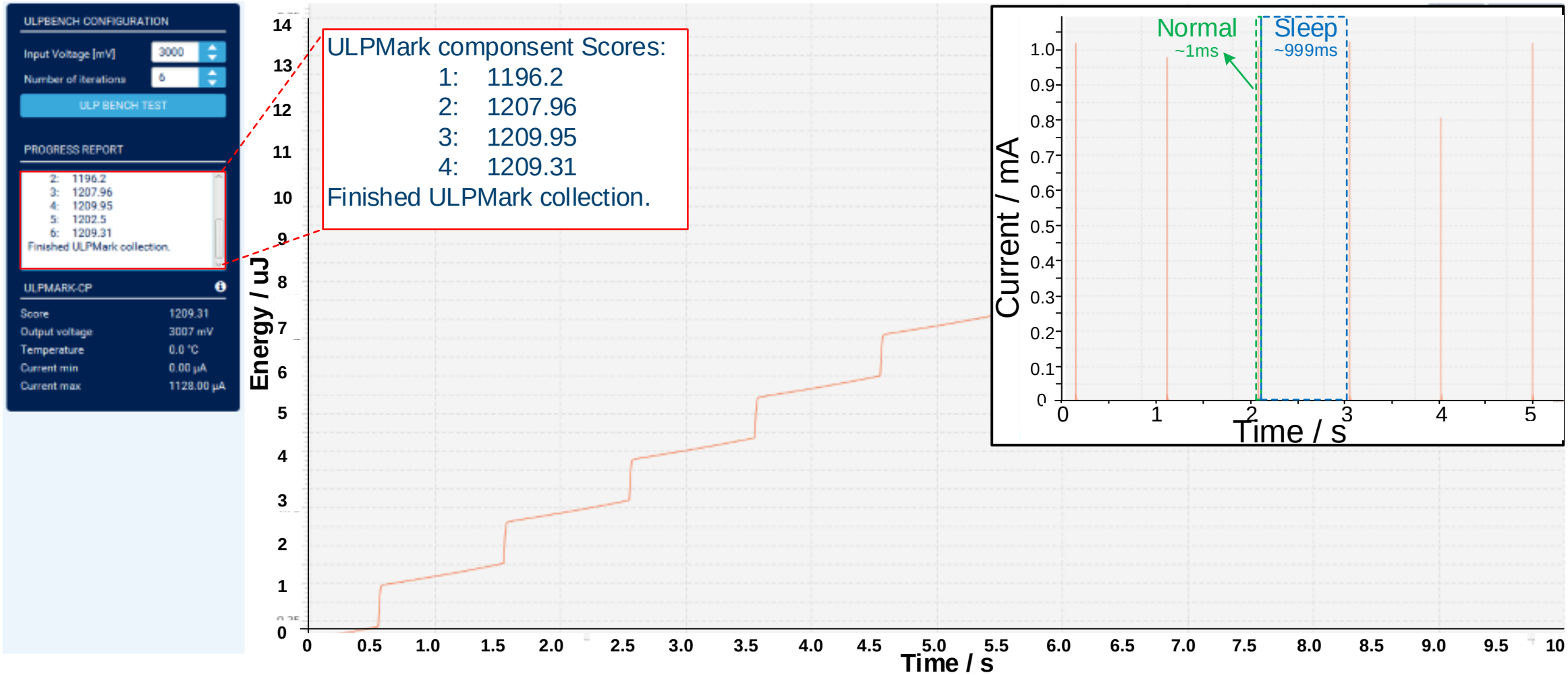
J-Link
Load programs to MCU

Energy Monitor
Power supply and signal acquisition



Test Board
Carry the MCU chip

Measured ULPMark-CP Score



Performance Summary of Stacking MCU

	ON Semi. RSL10	Ambiq Apollo512-KBR	This paper	
Architecture	Flat	Flat	Flat	Flat/Stack Dynamic Switching
Process	55nm	40nm	40nm	40nm
Voltage	3V	3V	3V	3V
Frequency	24MHz@run 32KHz@sleep	24MHz / 1MHz@run 32KHz@sleep	24MHz@run 32KHz@sleep	24MHz@run 32KHz@sleep
CPU	32-bits ARM Cortex-M3	32-bits ARM Cortex-M4	32-bits ARM Cortex-M3	32-bits ARM Cortex-M3
SRAM size@sleep	8KB	8KB	8KB	8KB
I/O	I2C / UART / SPI	I2C / UART / SPI	I2C / UART / SPI	I2C / UART / SPI
Sleeping Current	N/A	369nA@3V	170nA@3V	115nA@3V ★
ULPMark Score	1090	378	920	1205 ★

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Conclusions

- A dynamic voltage stacking scheme presented
  - Flat mode at active state
  - Stack mode at sleep state
- Protection circuits for avoiding too low effective supply voltage
  - A DRV protection unit for memories
  - A XO32 protection unit for XO32 and RTC logic
- A 40nm MCU chip is verified and achieves:
  - 170nA sleep current and 920 ULPMark-CP score @ flat architecture
  - 115nA sleep current and 1205 ULPMark-CP score @ dynamic voltage stacking architecture

Acknowledgements

Thank you for your kind attention

Acknowledgements

National Key Research and Development Project (No. 2018YFB2202001)

Proplus NanoYield™