An Ultra-Low-Jitter Frequency Synthesizer with Robust Lock Acquisition Performance

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2022年6月23日

Outline

- **Motivation and Background**
- **Proposed Integer-N TAPFD-based CPPLL**
  - The concept of TAPFD
  - Challenge for the implementation of TAPFD
  - Overall structure of the Proposed PLL
- **Measurement Results**
- **Conclusion**

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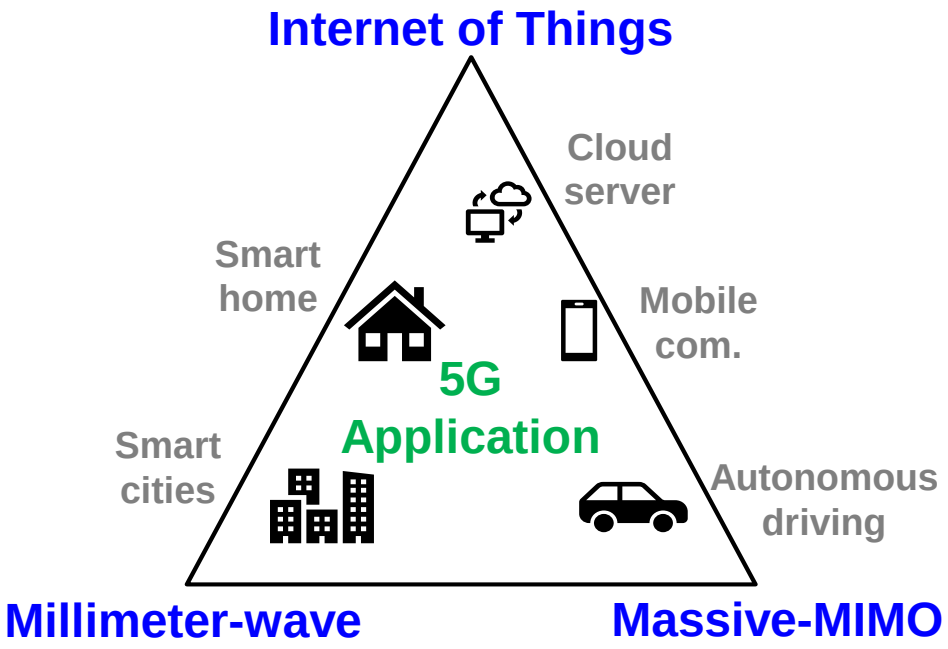
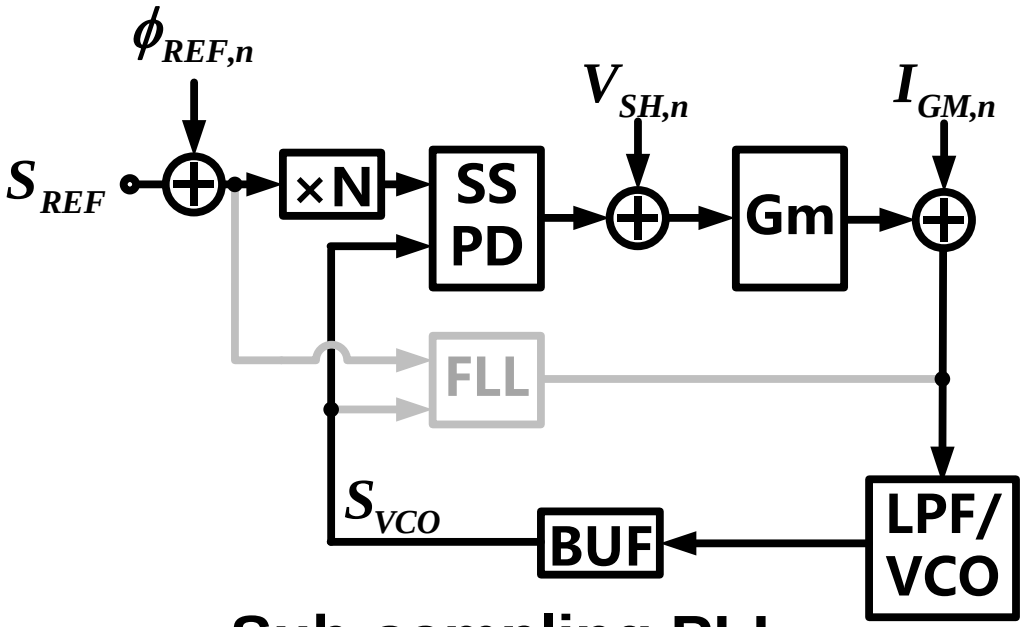
Demand for PLL in 5G Application



- Internet of Things
  - Low power consumption
- Millimeter-wave Communication
  - For 5G NR n258: 24.25GHz-27.5GHz
- Massive-MIMO
  - Ultra-low Jitter

Prior Arts with sub-100fs Jitter

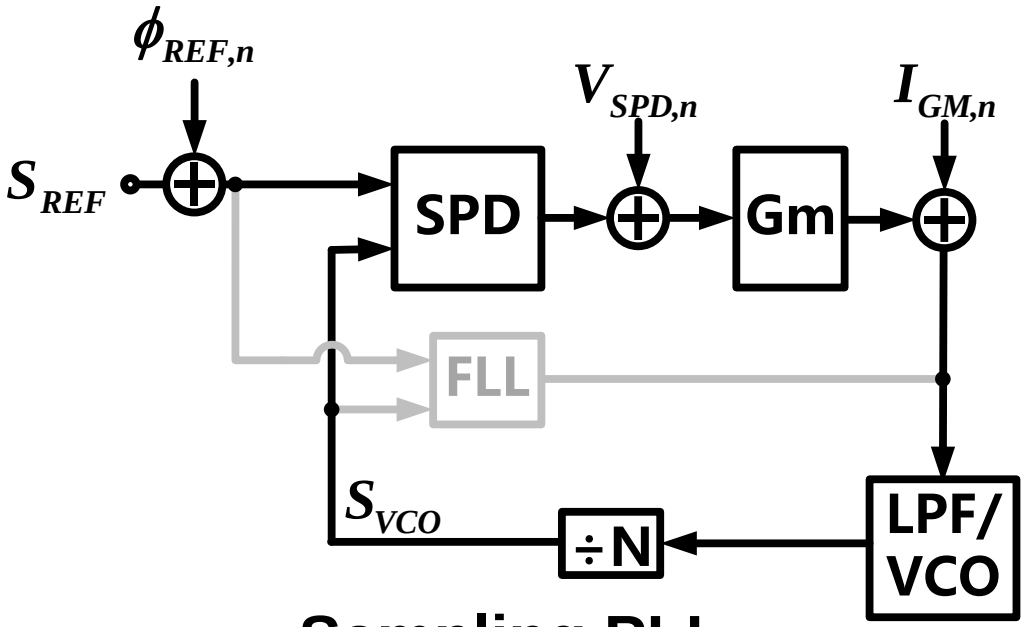


Sub-sampling PLL

[S. Lee, RFIC 19]

In-band noise referred to input:

$$\phi_{Inband2REF,n} = \left(V_{SH,n} + \frac{I_{GM,n}}{g_m}\right) / (K_{SSPD} \cdot N)$$



Sampling PLL

[W. Wu, ISSCC 21]

In-band noise referred to input:

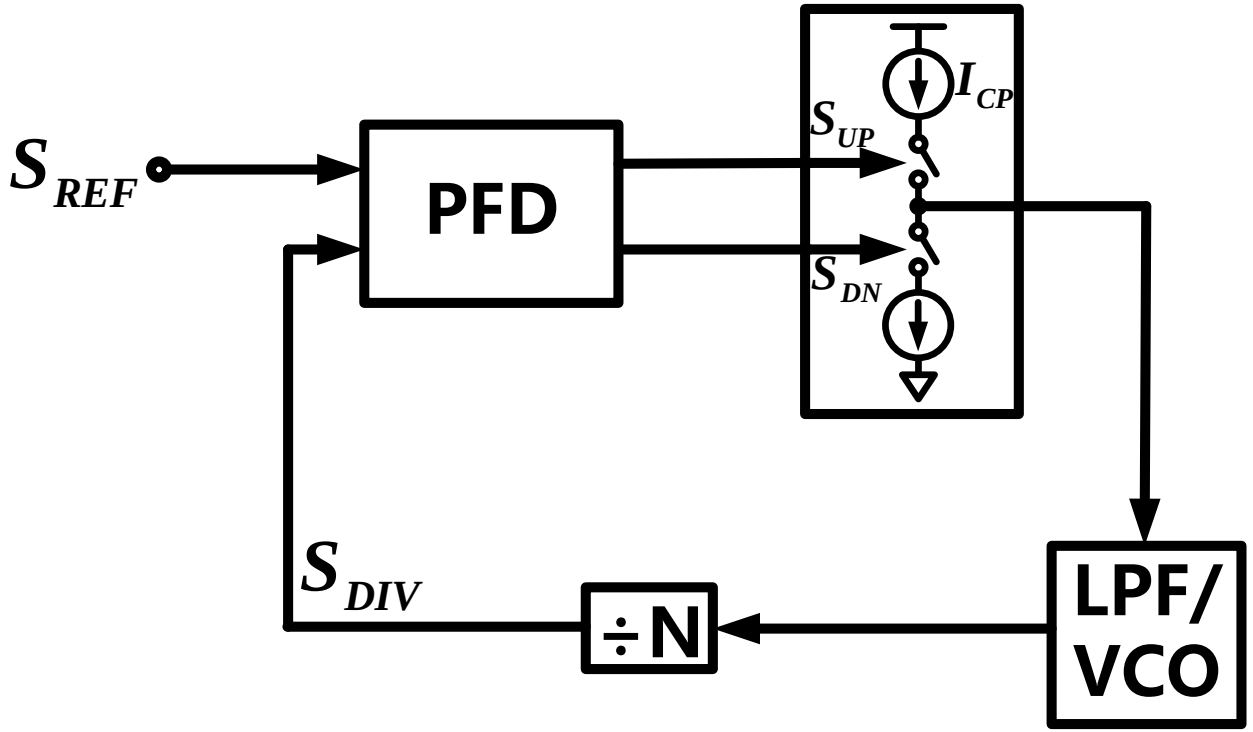
$$\phi_{Inband2REF,n} = \left(V_{SPD,n} + \frac{I_{GM,n}}{g_m}\right) / K_{SPD}$$

☺ **Input-referred noise of SSPD/SPD and Gm is greatly suppressed**

☹ **Lack of frequency detection results in a limited lock acquisition performance**

Is there any way to obtain robust lock acquisition and low in-band phase noise simultaneously?

Review: Conventional CPPLL

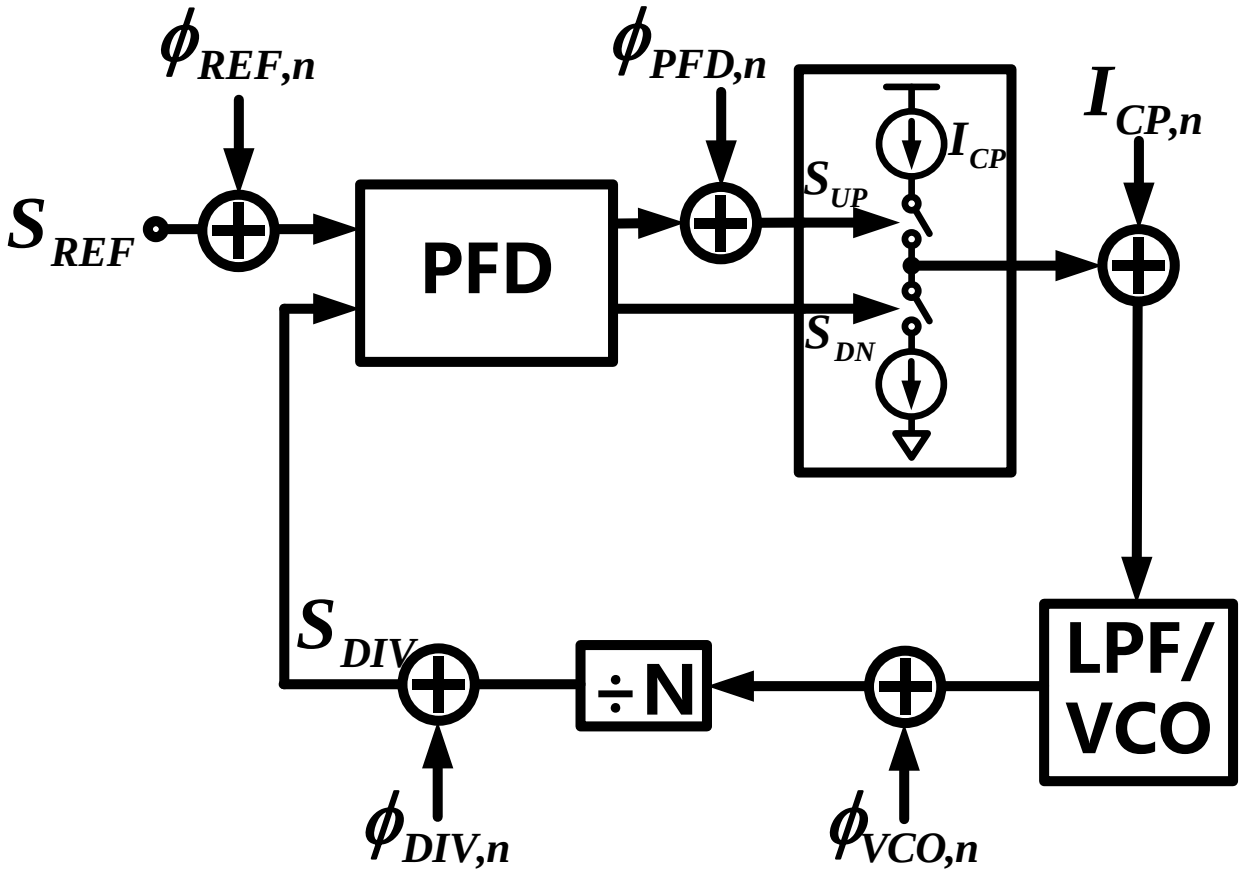


Conceptual Block Diagram of Conventional CPPLL

☺ **Freq. detection capability, avoiding potential long relock time**

☹ **CP dominates in-band noise, thus poor in-band phase noise**

Review: Noise in Conventional CPPLL



Conventional CPPLL Block Diagram w/ Noise Source

- $\phi_{PFD,n}$ and $\phi_{DIV,n}$ are negligible
- Input-referred noise of CP:

$$\phi^2_{CP2REF,n} = \left(\frac{2\pi}{I_{CP} \cdot K_{PFD}}\right)^2 I^2_{CP,n}$$

- For 1/f noise within PLL bandwidth:

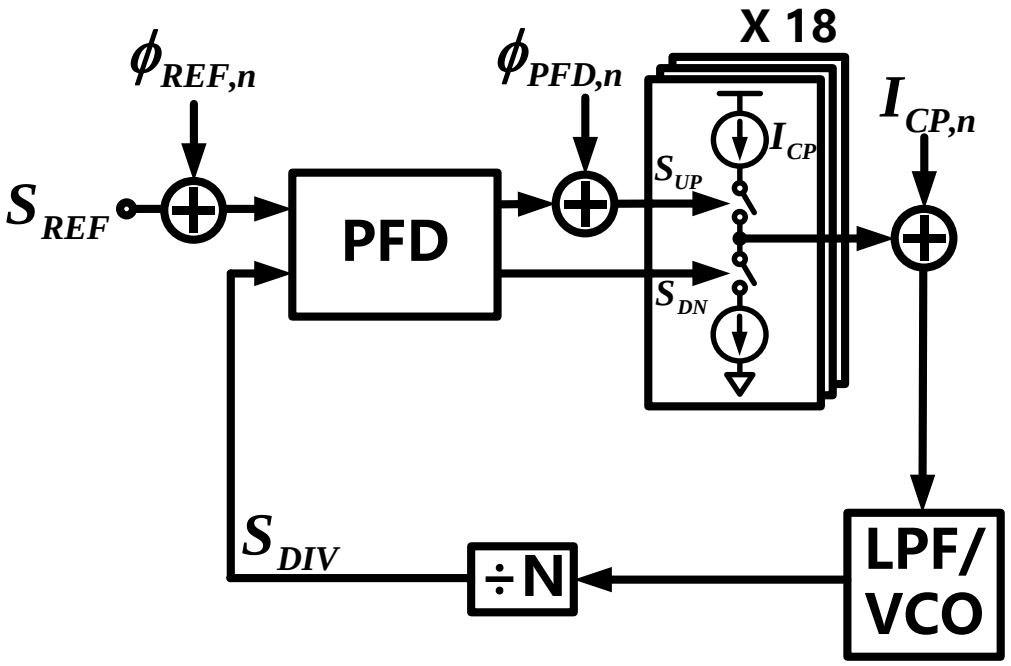
$$I^2_{CP,n} \propto I_{CP}$$

- Thus,

$$\phi^2_{CP2REF,n} \propto \frac{1}{I_{CP}}$$

Power ⟷ Noise (Tradeoff)

Prior Arts with sub-100fs Jitter



Charge Pump PLL

[D. Turker, ISSCC 18]

In-band noise referred to input:

$$\phi_{Inband2REF,n} = \phi_{PFD,n} + \frac{2\pi \cdot I_{CP,n}}{18 \cdot I_{CP}}$$

- **18 CP unit slices in parallel**
  - ☺ – Increase CP current
  - ☹ – High Power (45mW in total)
- **30~40ps CP deadzone pulse width**
  - ☺ – Minimize CP ON-state duty cycle
  - ☹ – Advanced process (16nm-FinFET)

Power-Noise Tradeoff in CPPLL

Conventional PFD+CP → $\phi^2_{CP2REF,n} \propto \frac{1}{I_{CP}}$ → 2x Power -3dB PN

New CPPLL Structure? → Suppress the CP Noise → Break the Tradeoff

How to break the power-noise tradeoff in CP?

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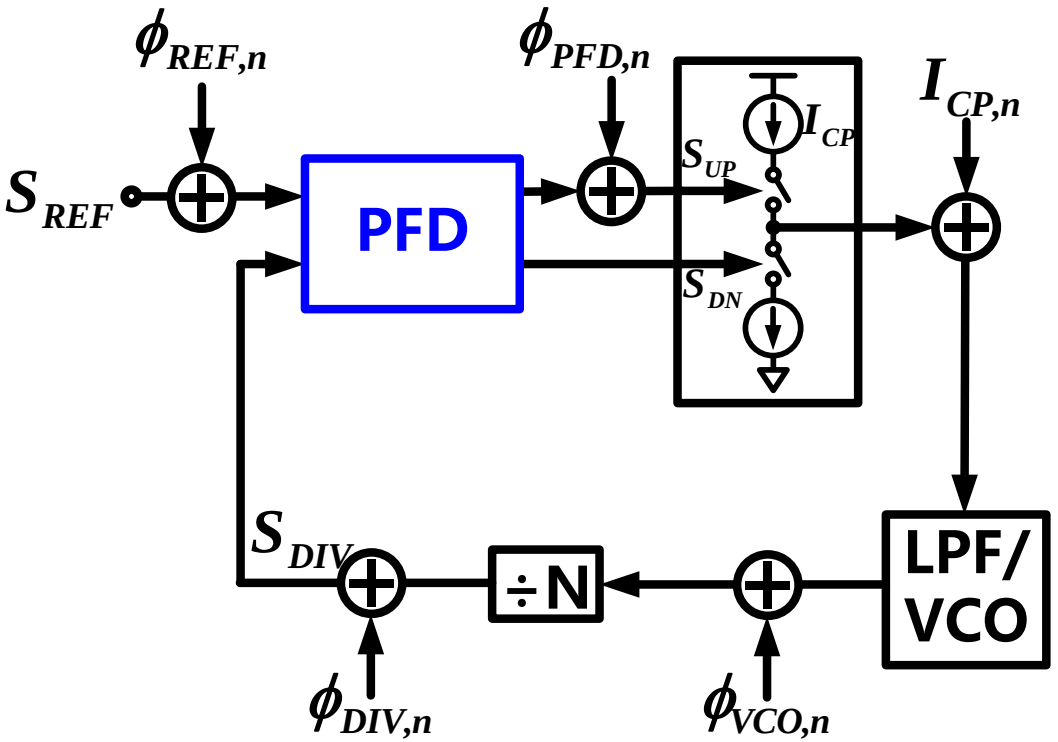
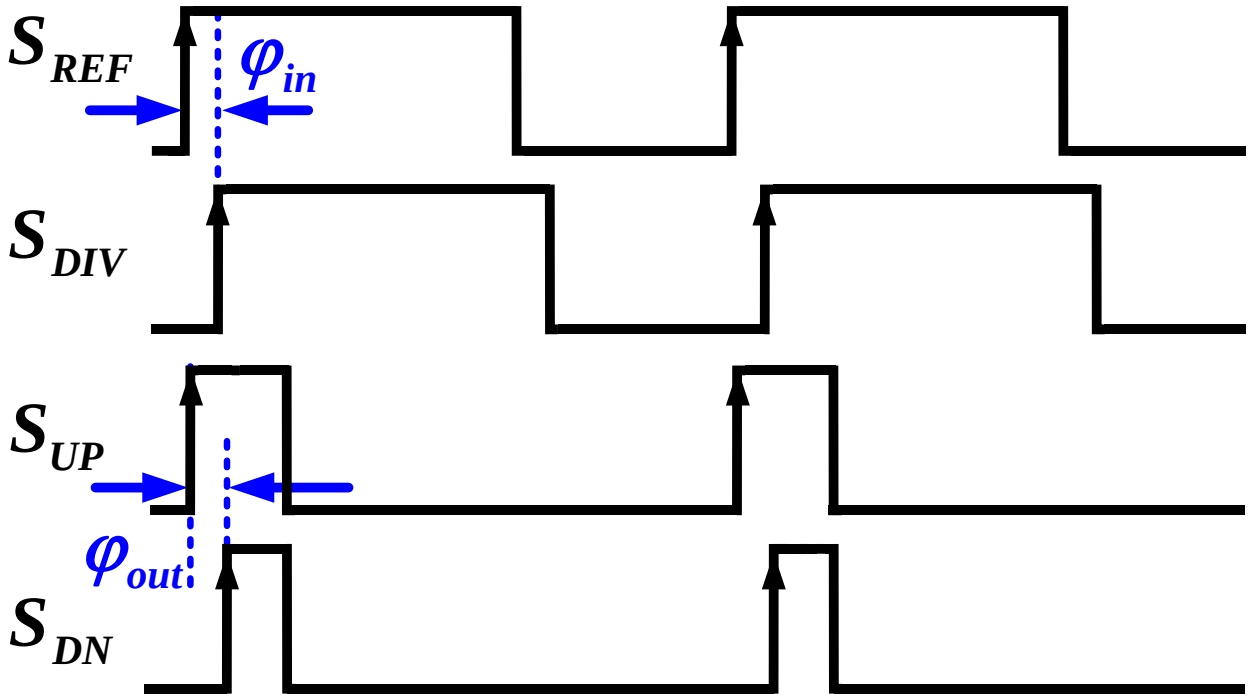
The Concept of Conventional PFD



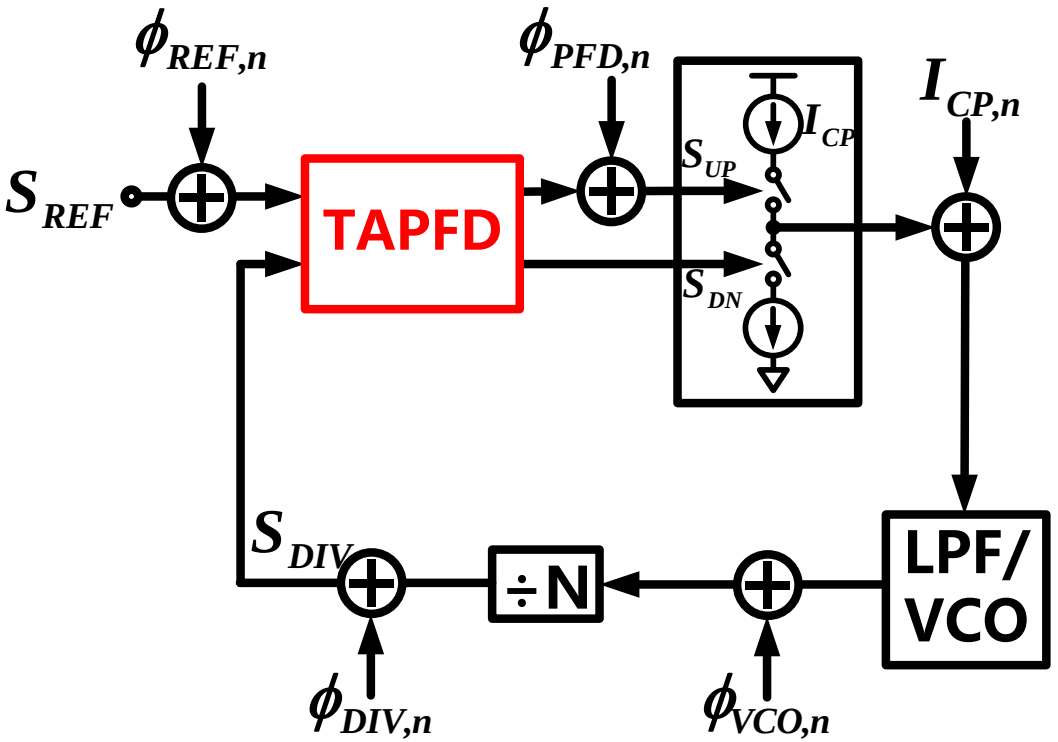
CPPLL Block Diagram



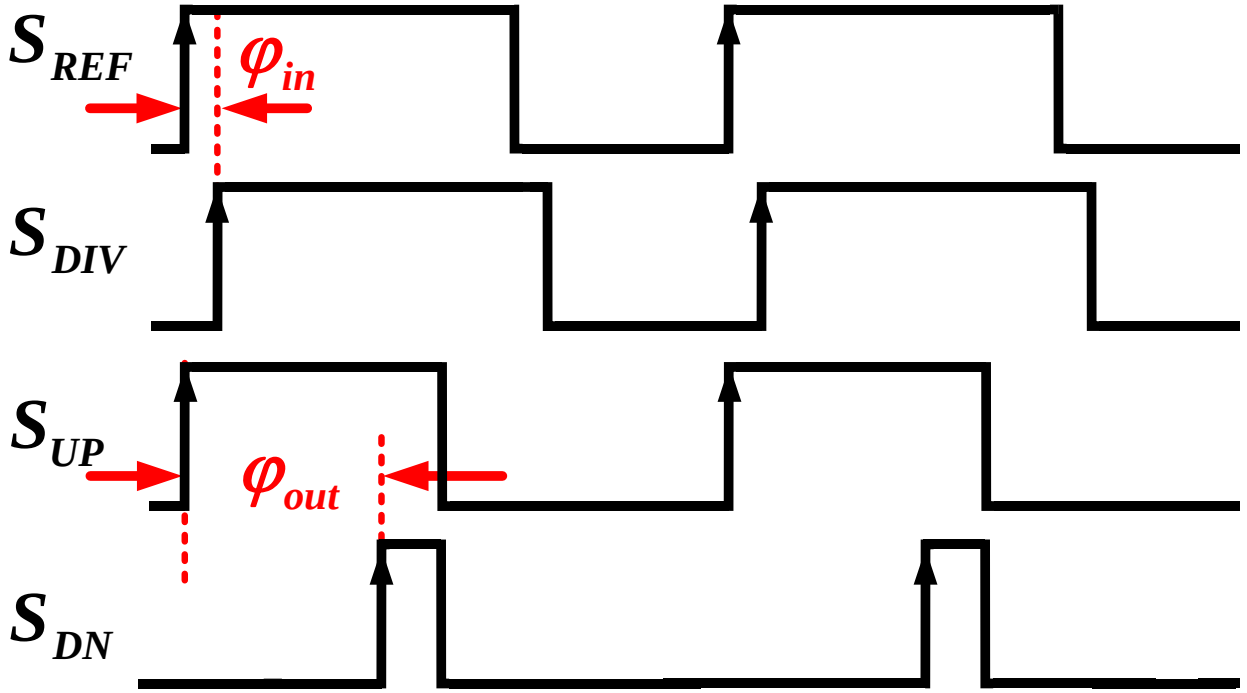
Conventional PFD Timing Diagram

- PFD gain: $K_{PFD} = \varphi_{out}/\varphi_{in} = 1$
- Input-referred noise of CP: $\phi^2_{CP2REF,n} = \left(\frac{2\pi}{I_{CP} \cdot K_{PFD}}\right)^2 I^2_{CP,n}$

The Concept of TAPFD



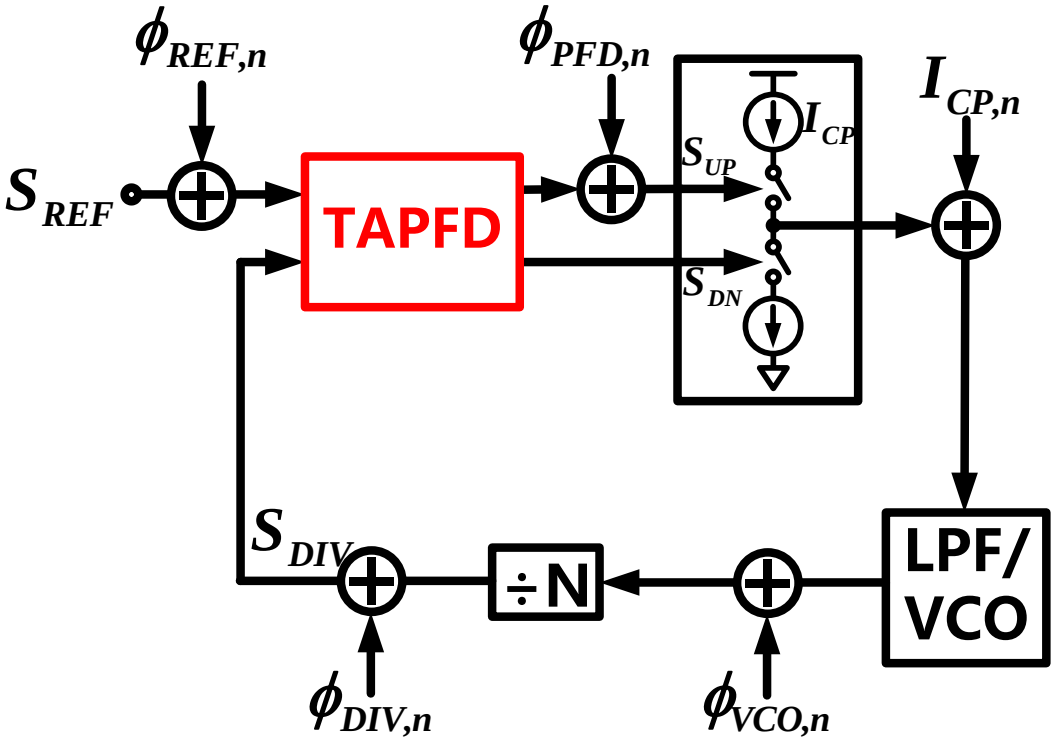
CPPLL with TAPFD Block Diagram



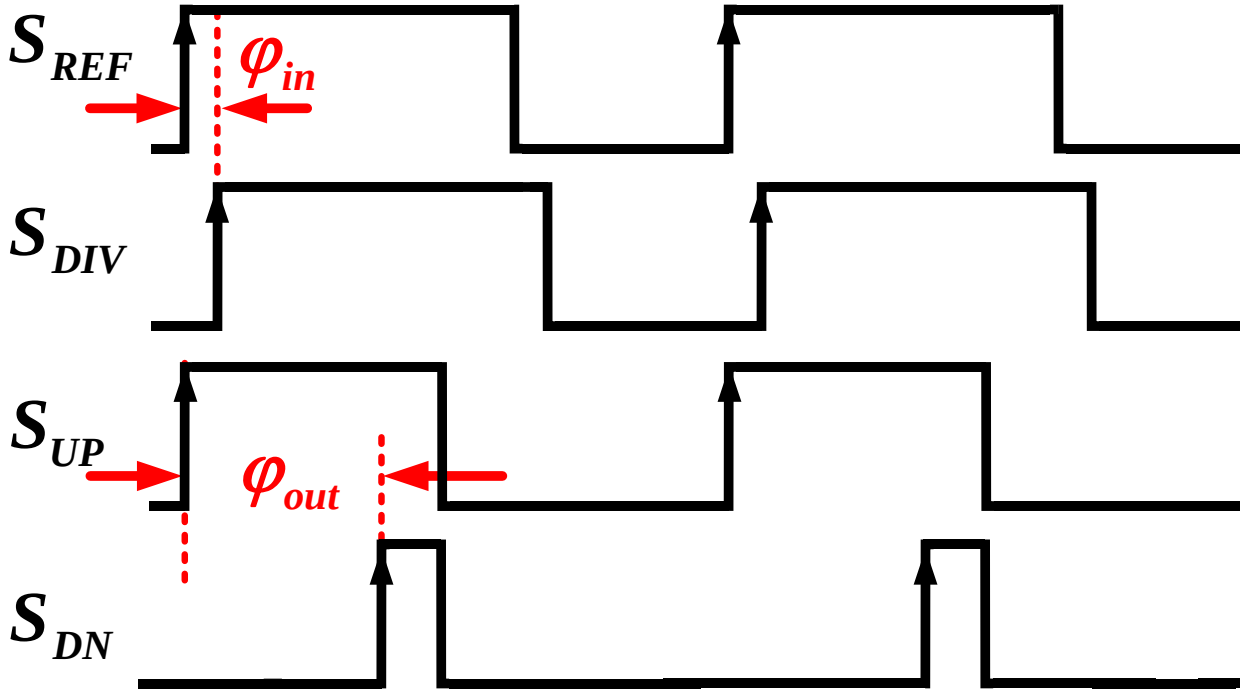
Time-amplifying PFD (TAPFD) Timing Diagram

- TAPFD gain: $K_{TAPFD} = \varphi_{out}/\varphi_{in} > 1$
- Input-referred noise of CP: $\phi^2_{CP2REF,n} = \left(\frac{2\pi}{I_{CP} \cdot K_{TAPFD}}\right)^2 I^2_{CP,n}$

The Concept of Proposed TAPFD



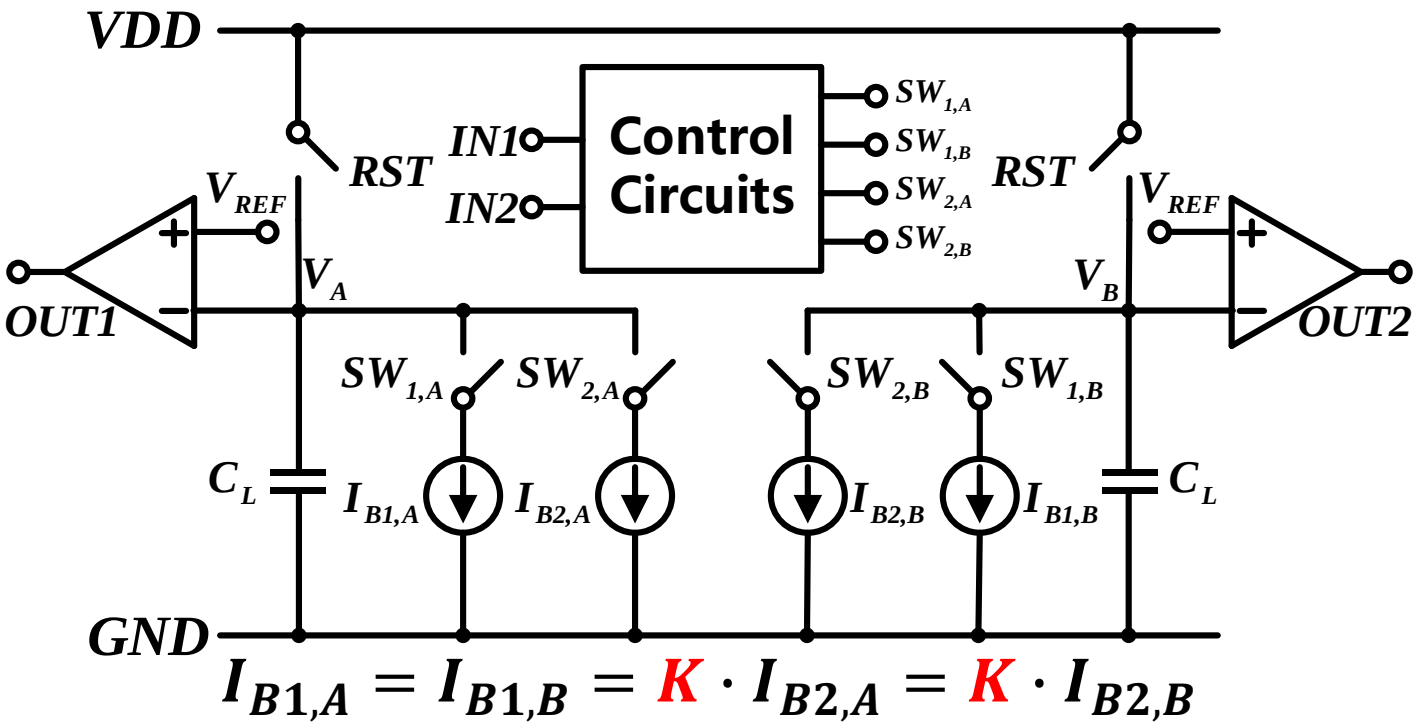
CPPLL with TAPFD Block Diagram



Time-amplifying PFD (TAPFD) Timing Diagram

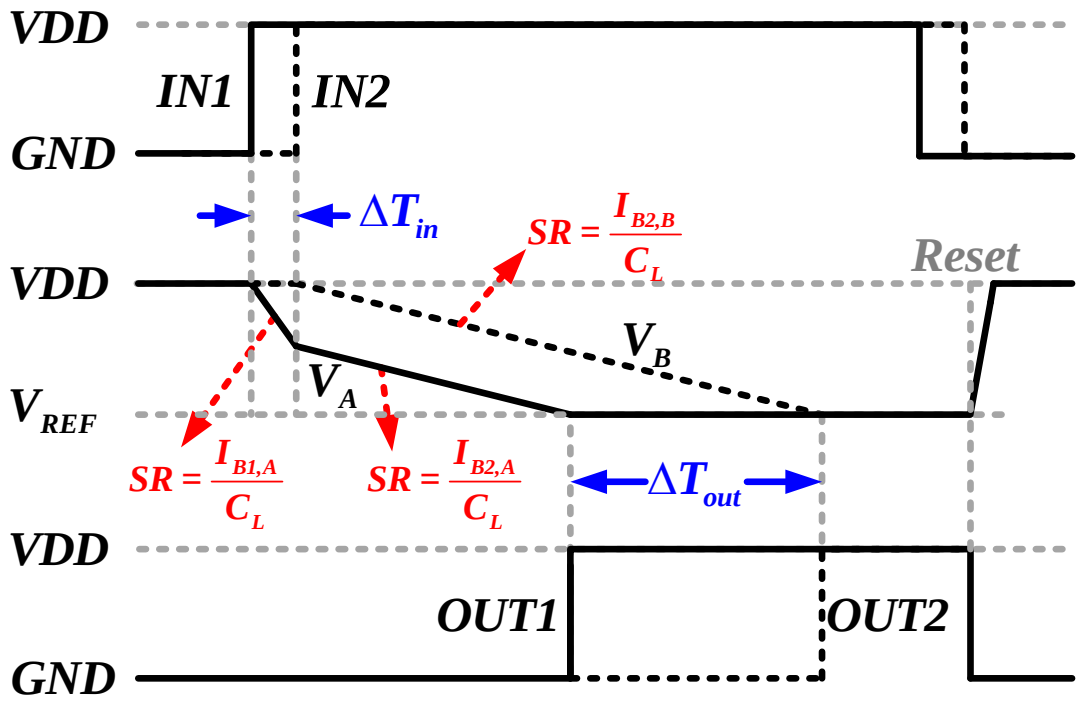
☺ Input-referred noise of CP is suppressed by K_{TAPFD}

The Realization of Time-Amplifying



$$I_{B1,A} = I_{B1,B} = K \cdot I_{B2,A} = K \cdot I_{B2,B}$$

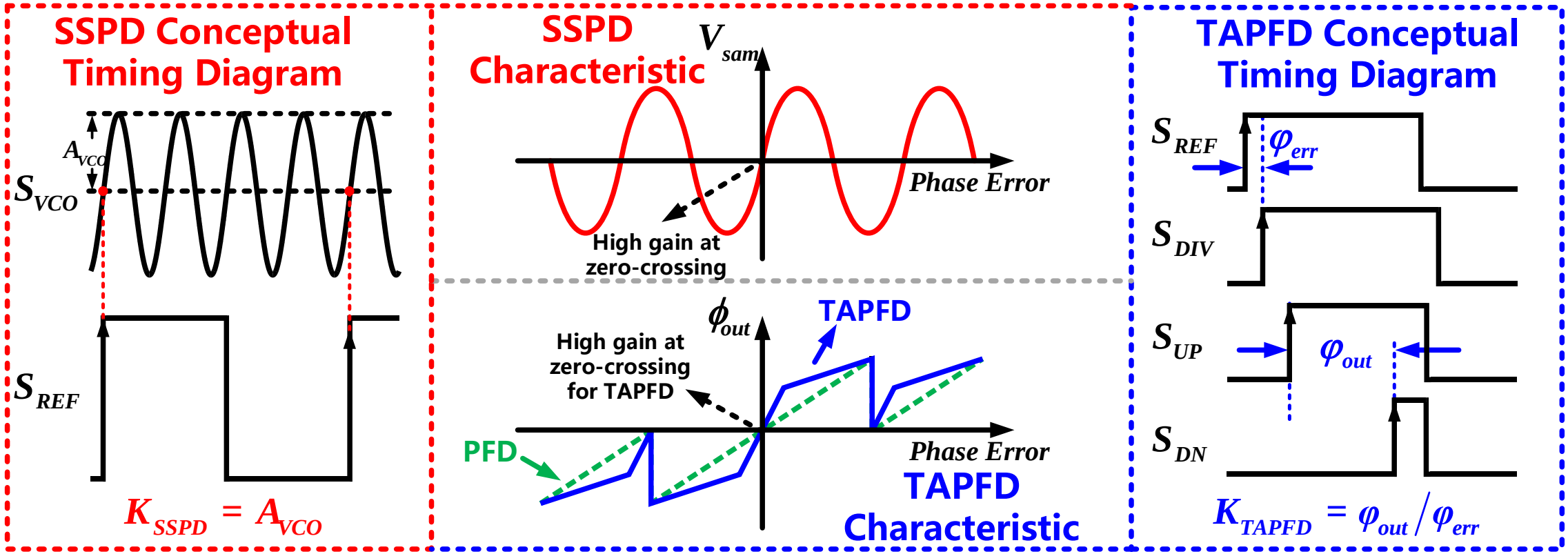
A typical Time Amplifier Diagram
[H. Kwon, TCAS-II 14]



Timing Diagram of TA

◆ The discharging current ratio determines the amplification gain: $\frac{\Delta T_{out}}{\Delta T_{in}} = K$

Transfer Characteristic of TAPFD



- TAPFD maintains the frequency detection capability as PFD
- TAPFD can obtain high phase-error gain at zero-crossing as SSPD/SPD

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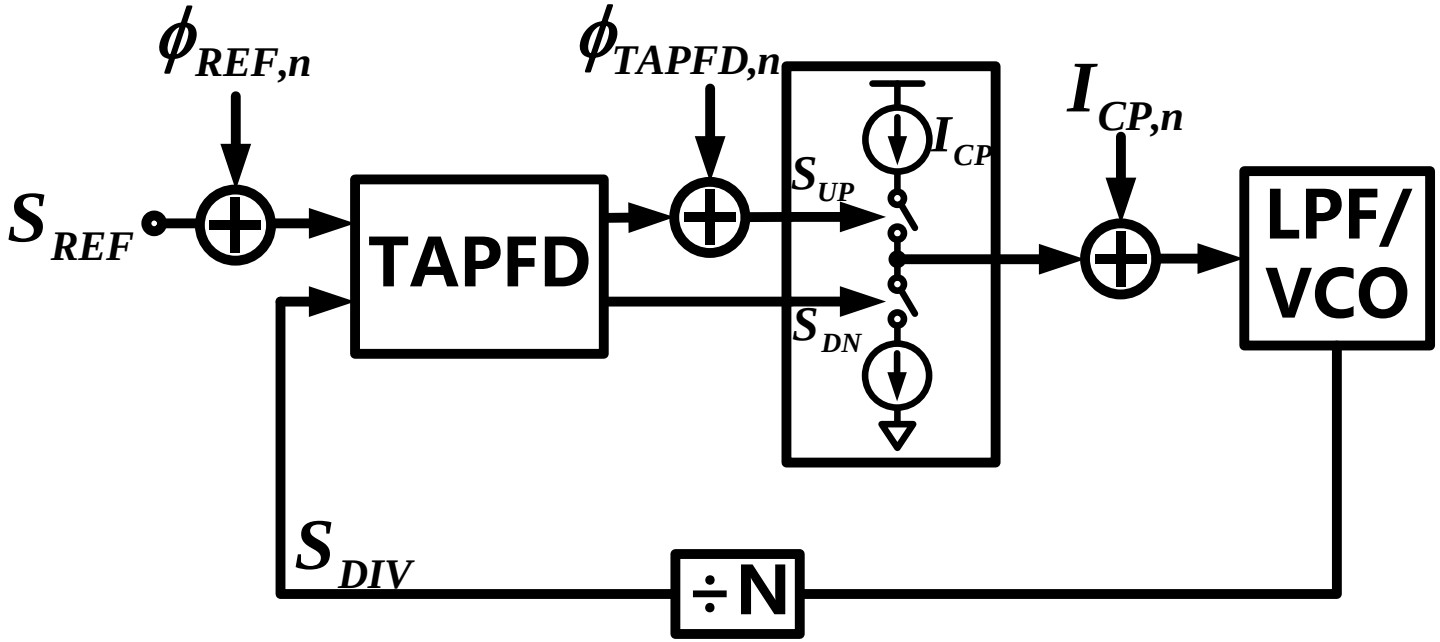
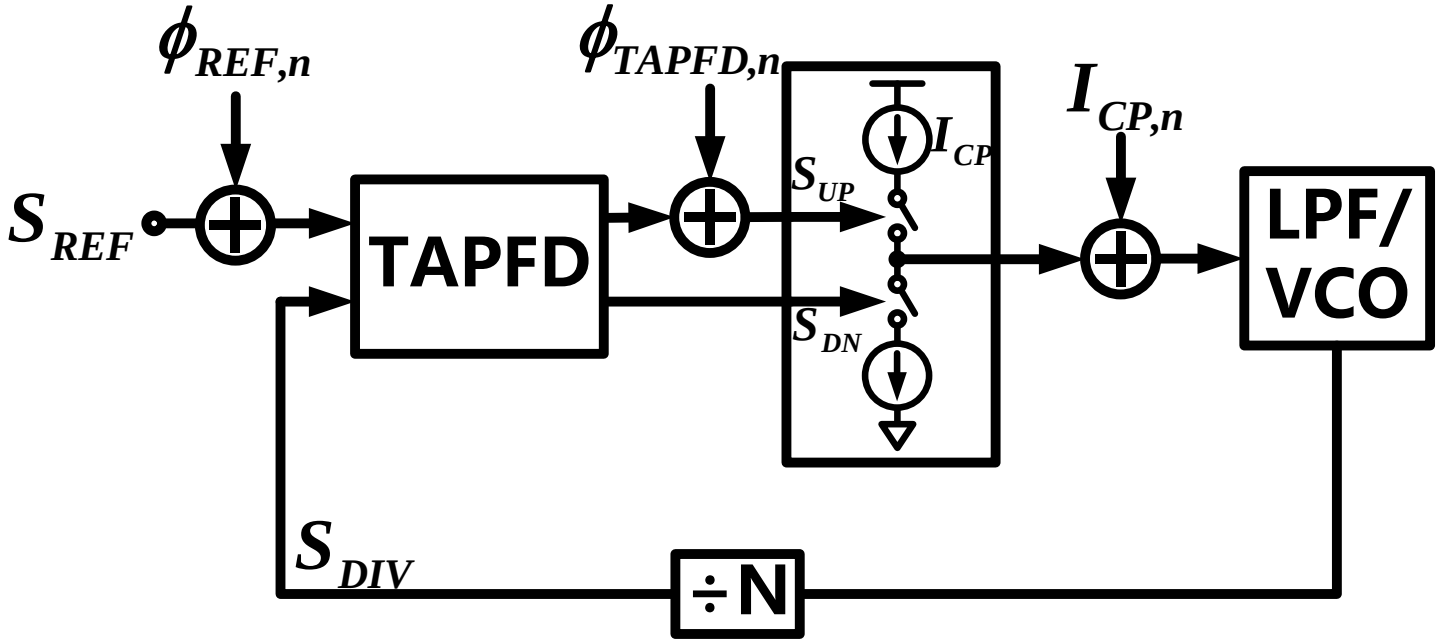
Noise in TAPFD



TA-CPPLL Block Diagram with Noise Source

- **TAPFD could contribute to input-referred noise**
- **Once it's too large, it can severely degrade in-band phase noise**

Noise in TAPFD



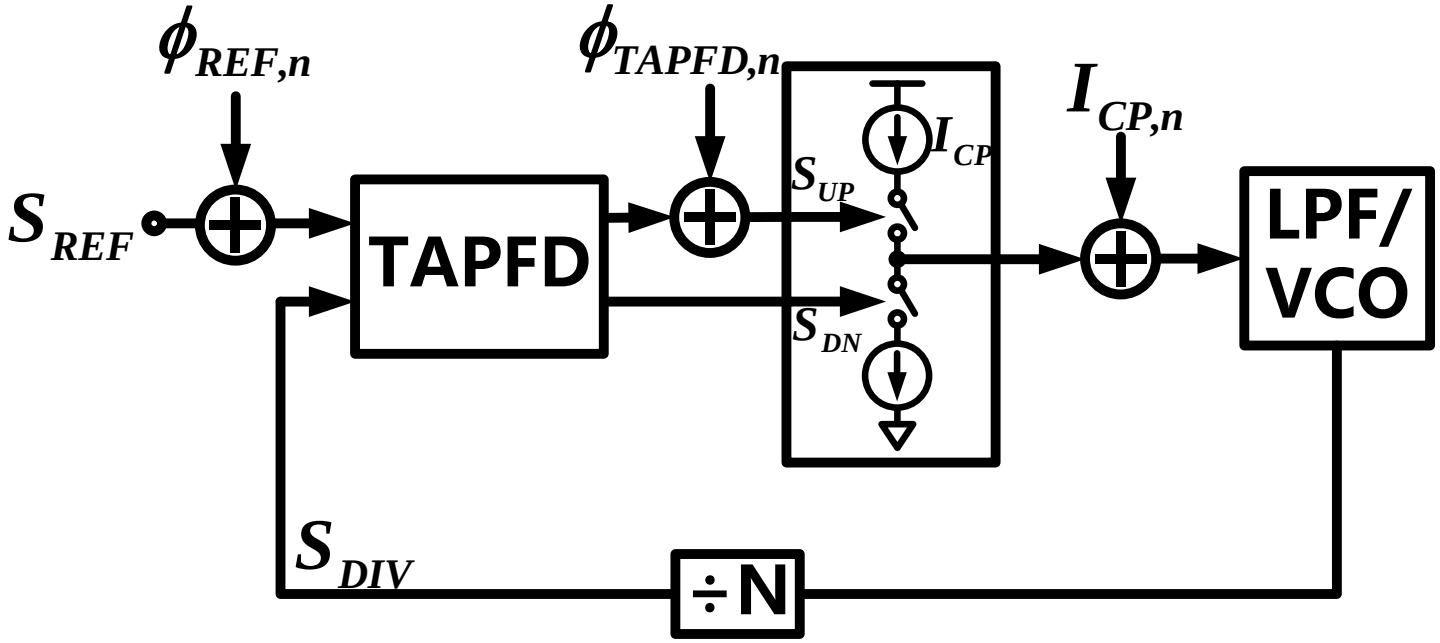
TA-CPPLL Block Diagram with Noise Source

For example, if $\phi_{TAPFD,n}^2 = \left(K_{TAPFD}^2 - 1\right) \cdot \left(\frac{2\pi}{I_{CP}.}\right)^2 I_{CP,n}^2$, **then**

$$\phi_{Inband2REF,n}^2 = \left[\left(\frac{2\pi}{I_{CP}}\right)^2 I_{CP,n}^2 + \phi_{TAPFD,n}^2\right] \Big/ K_{TAPFD}^2 = \left(\frac{2\pi}{I_{CP}}\right)^2 I_{CP,n}^2$$

Equals to PFD/CP scheme

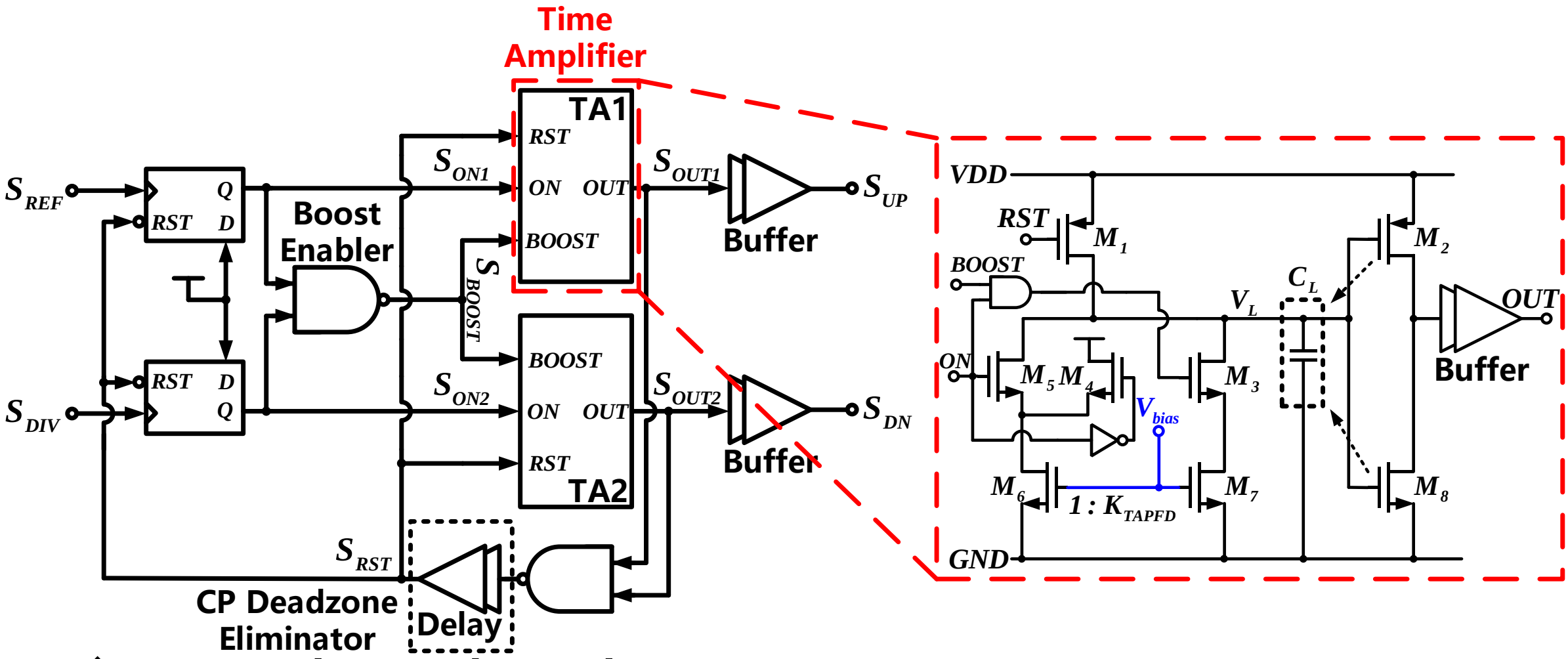
Challenge for the Design of TAPFD



TA-CPPLL Block Diagram with Noise Source

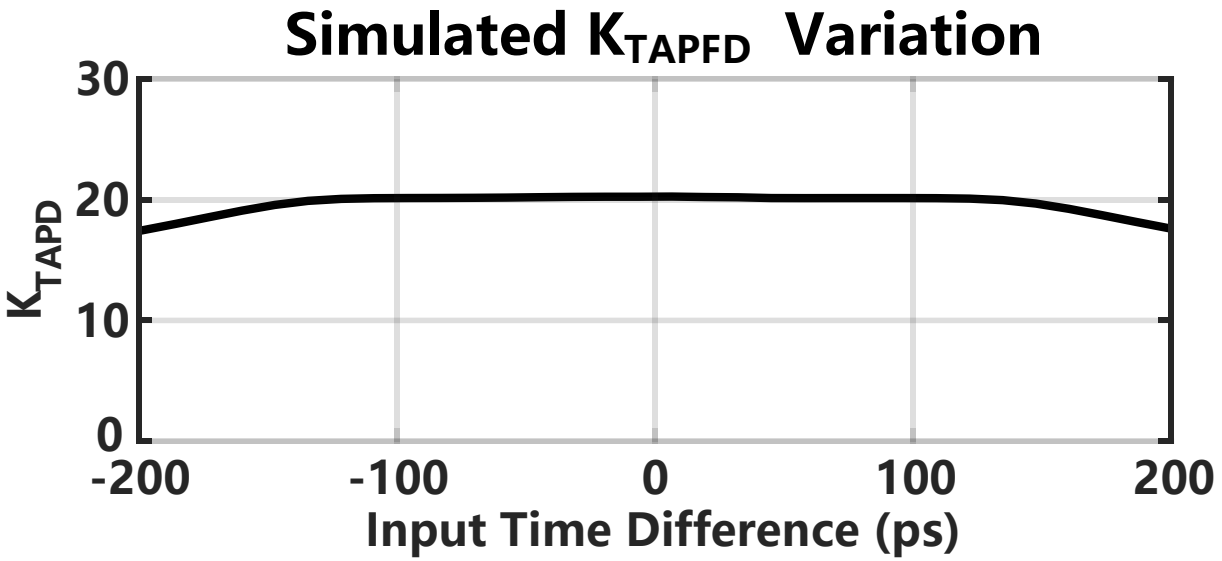
Challenge: Minimizing TAPFD phase noise to achieve effective noise suppression!

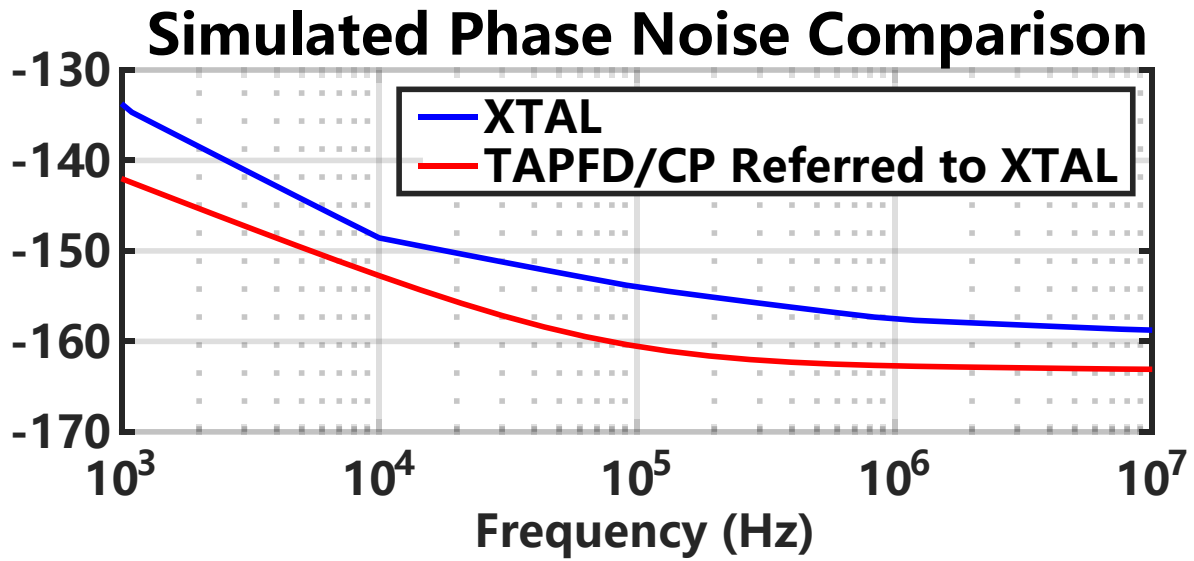
Detailed Implementation of TAPFD



- TA1 and TA2 share the same V_{bias}
- Thus the noise on V_{bias} can be cancelled by $S_{OUT1} - S_{OUT2}$

Simulation Results of TAPFD





- 20x Phase-error gain
- Linear range is +/- 150ps
- Input-referred phase noise is smaller than XTAL

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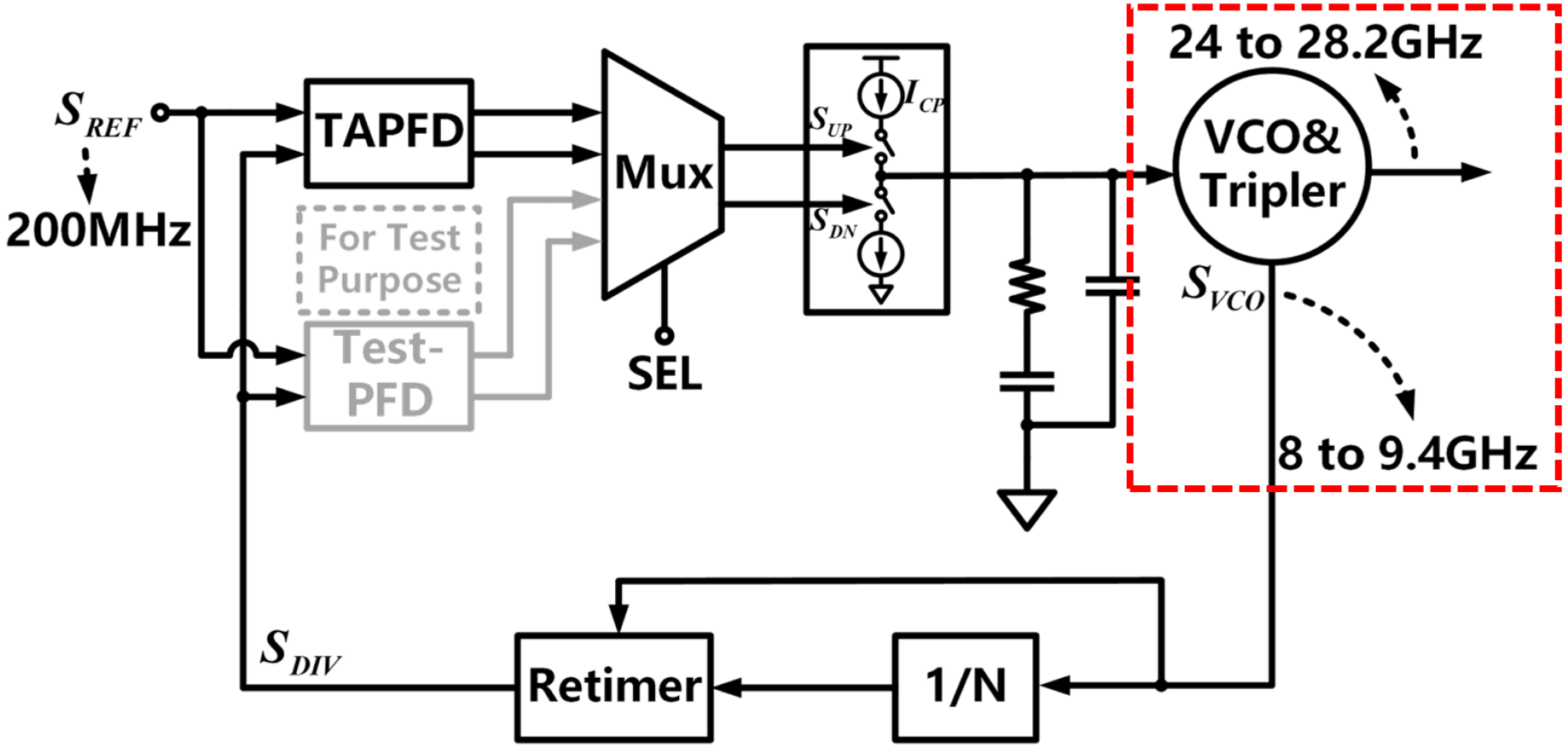
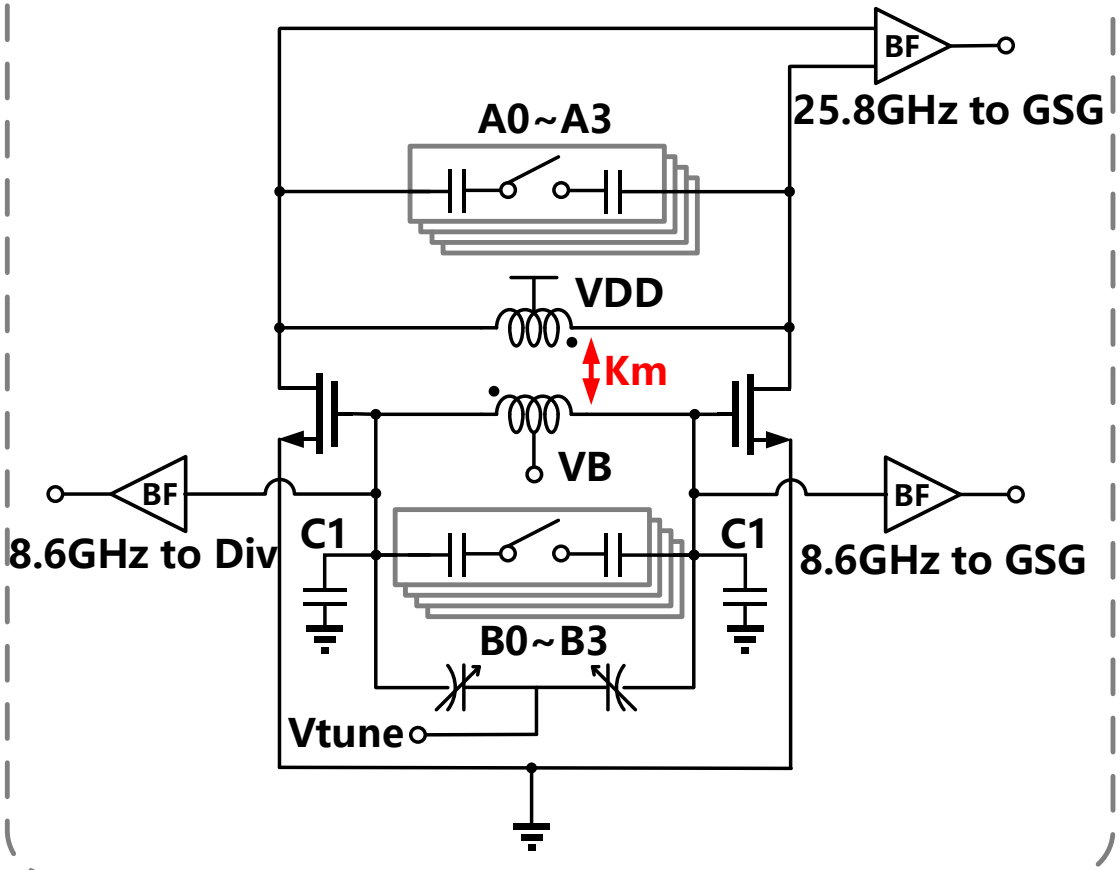
Overall Structure

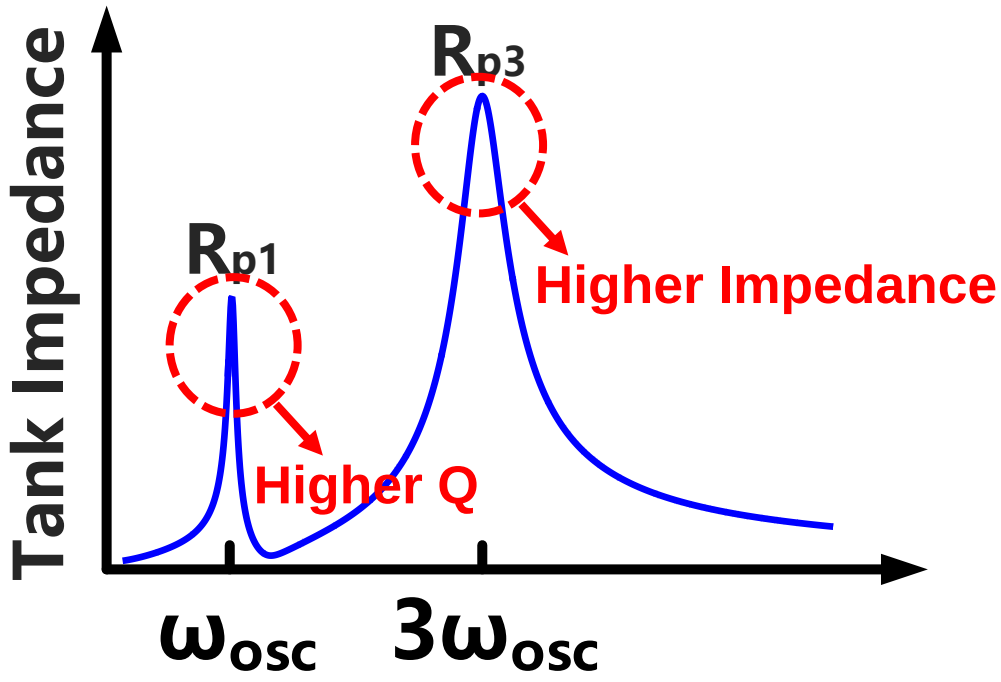


- A class-F VCO w/ built in tripler:
  - Feedback the fund. to relax divider/retimer operating frequency
  - The fund. LC tank achieves a better Q-factor than 3rd harmonic

Implementation of VCO

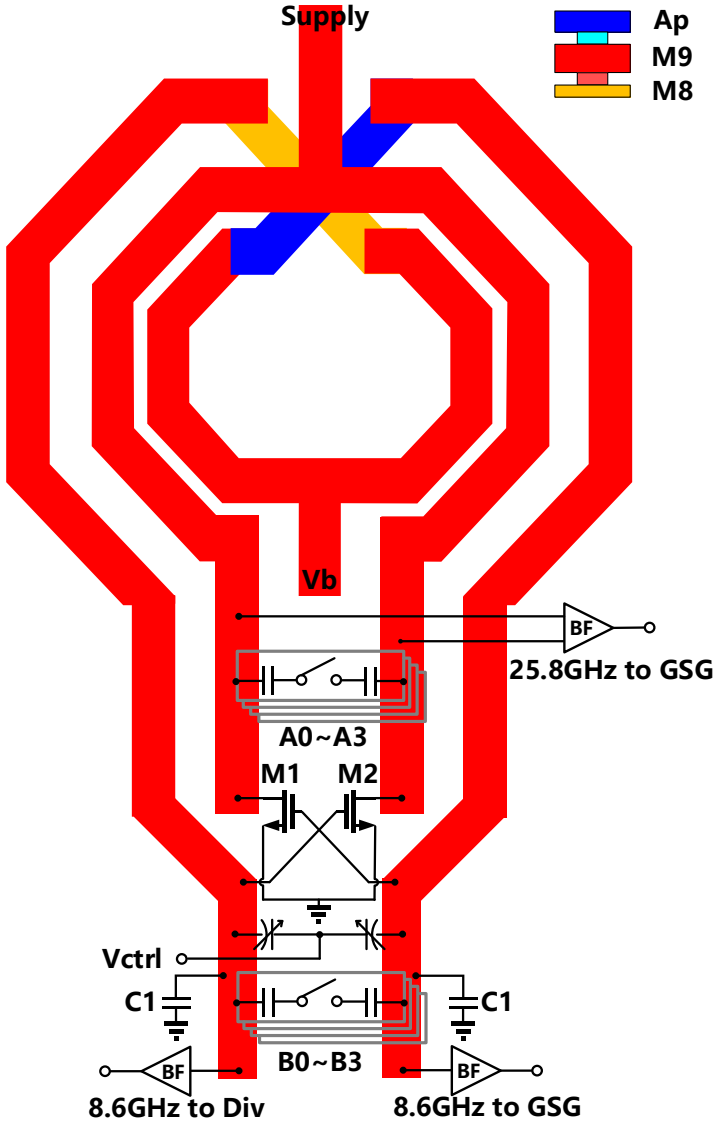
The Schematic of Class-F VCO with 3rd Harmonic Extraction





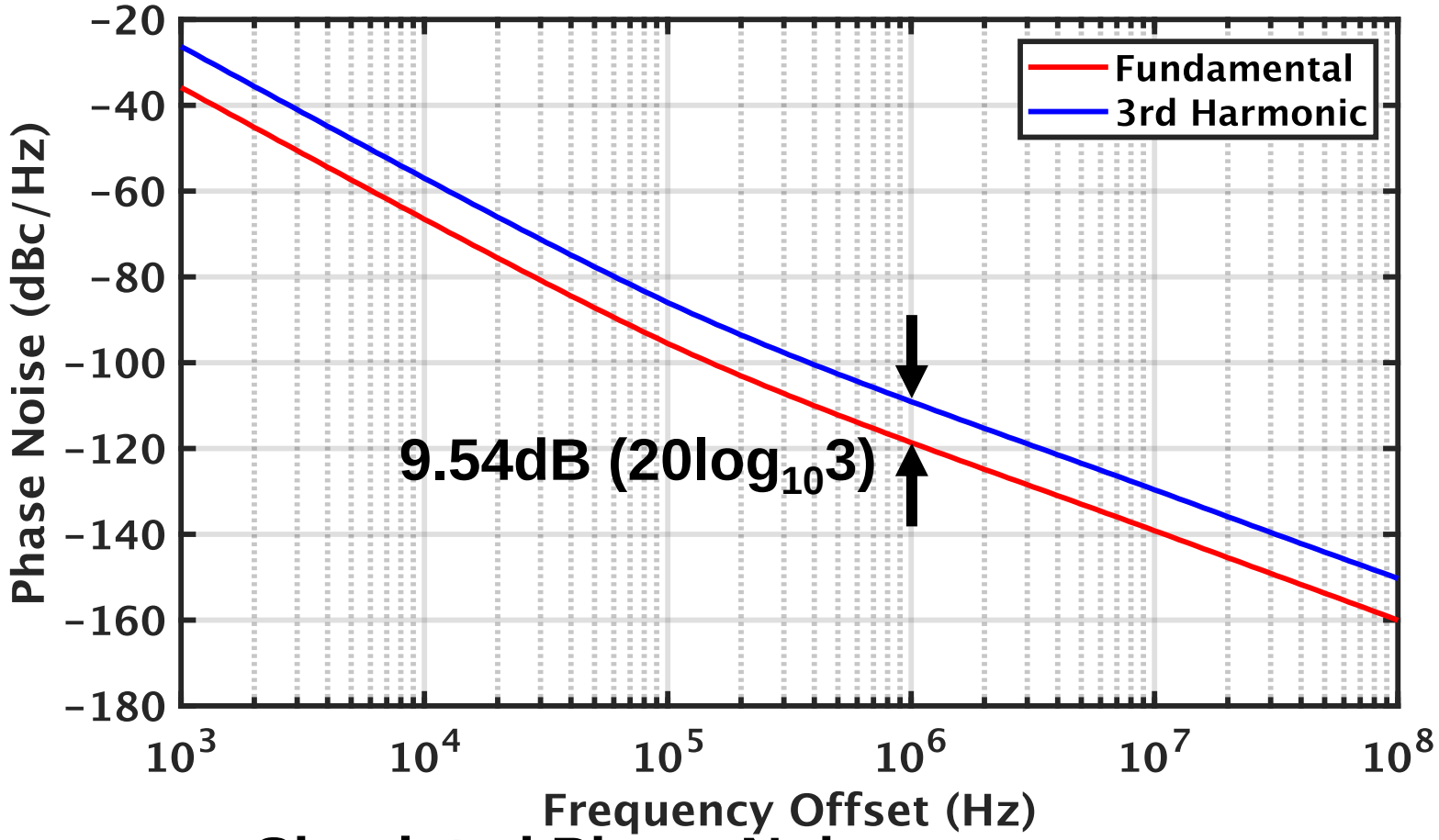
- Km=0.6 to tradeoff:
  - Q_{eq} at fund. for better PN
  - Third harmonic impedance to improve output swing

Layout of 3rd HE VCO



- Fully symmetrical layout for less mismatch
- 25.8GHz LC Tank is placed near M1,M2 to reduce EM loss
- Transformer is made of thick metal M9 at the same layer to maintain both high Q and enough Km

Simulated VCO Phase Noise



- **Simulated Phase Noise:**
  - **-118.6dBc/Hz@1MHz for fundamental**
  - **-109.1dBc/Hz@1MHz for 3rd harmonic**

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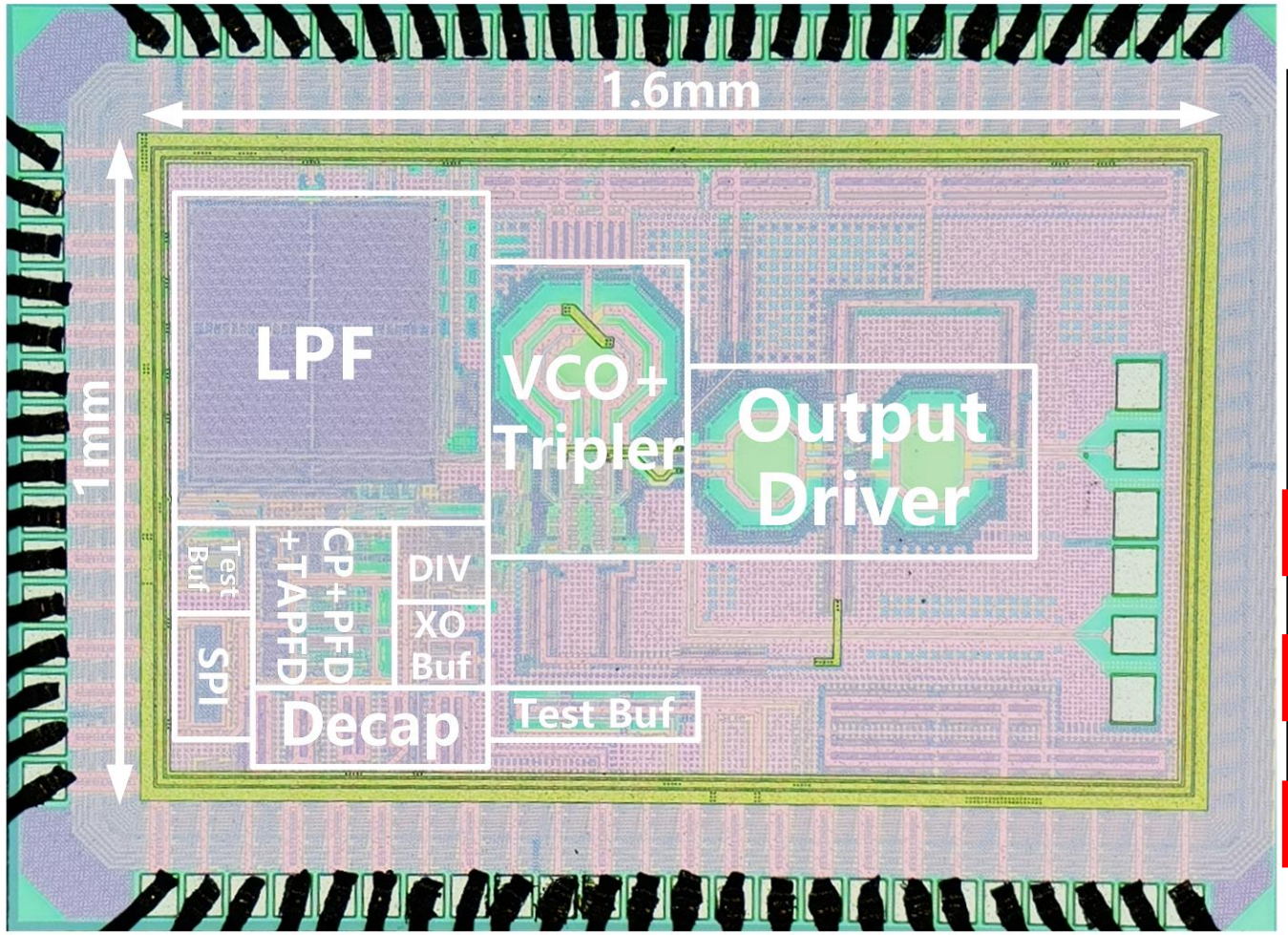
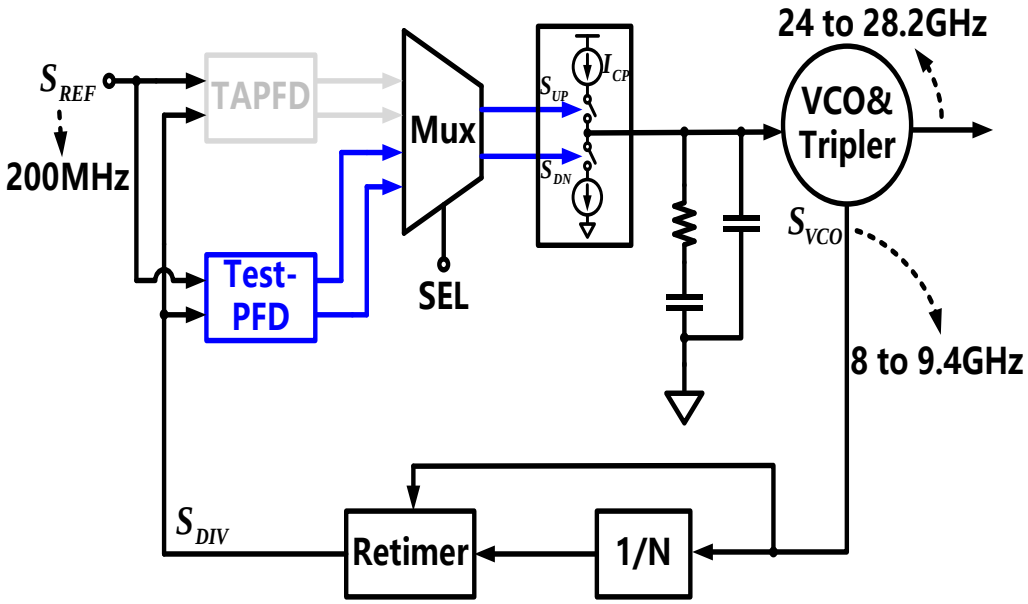
Chip Micrograph



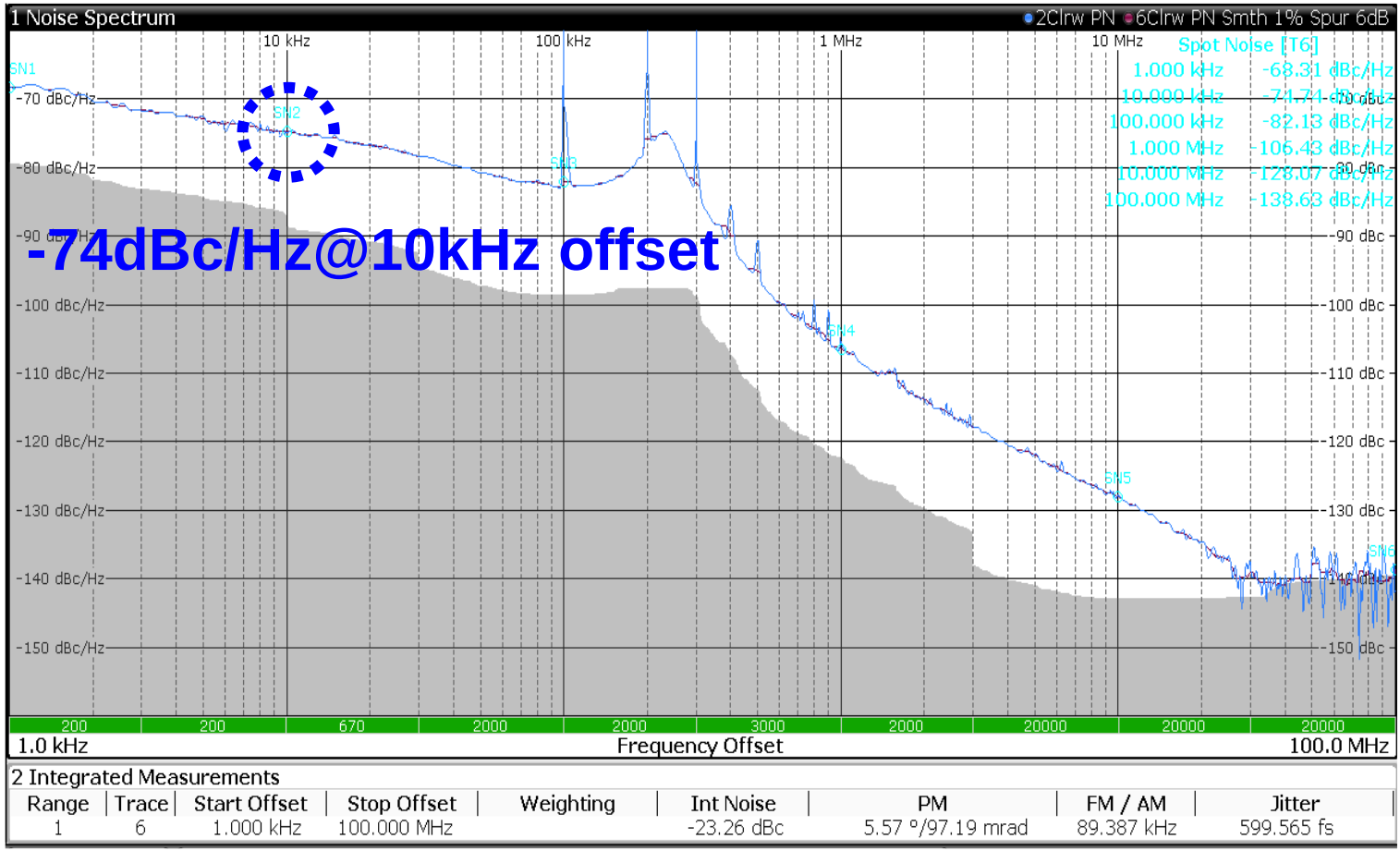
Blocks	Power (mW)	Area (mm^2)
LC VCO+ Tripler	11.47	0.13
Divider	1.12	0.03
XO Buf	NA	
TAPFD	1.07	0.05
PFD	NA	
CP	0.82	
LPF	NA	0.24
Total	14.48	0.45

- 65nm CMOS
- Ref. Freq.: 200MHz
- Out. Range: 24 to 28.2GHz
- Core Area: 0.45mm^2
- Power: 14.48mW

Measured Phase Noise

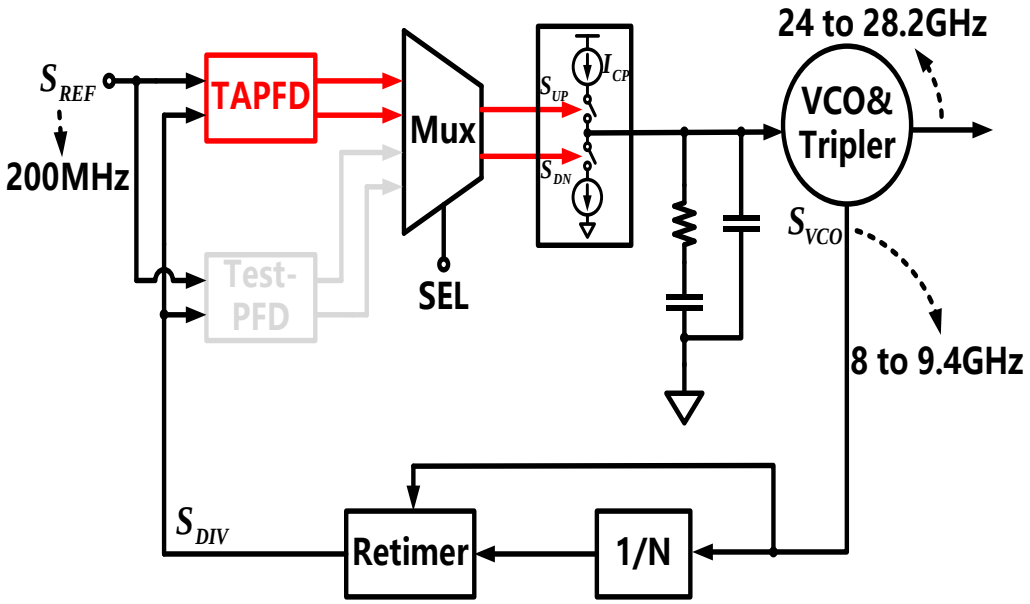


Measured PN w/ Test-PFD in Charge

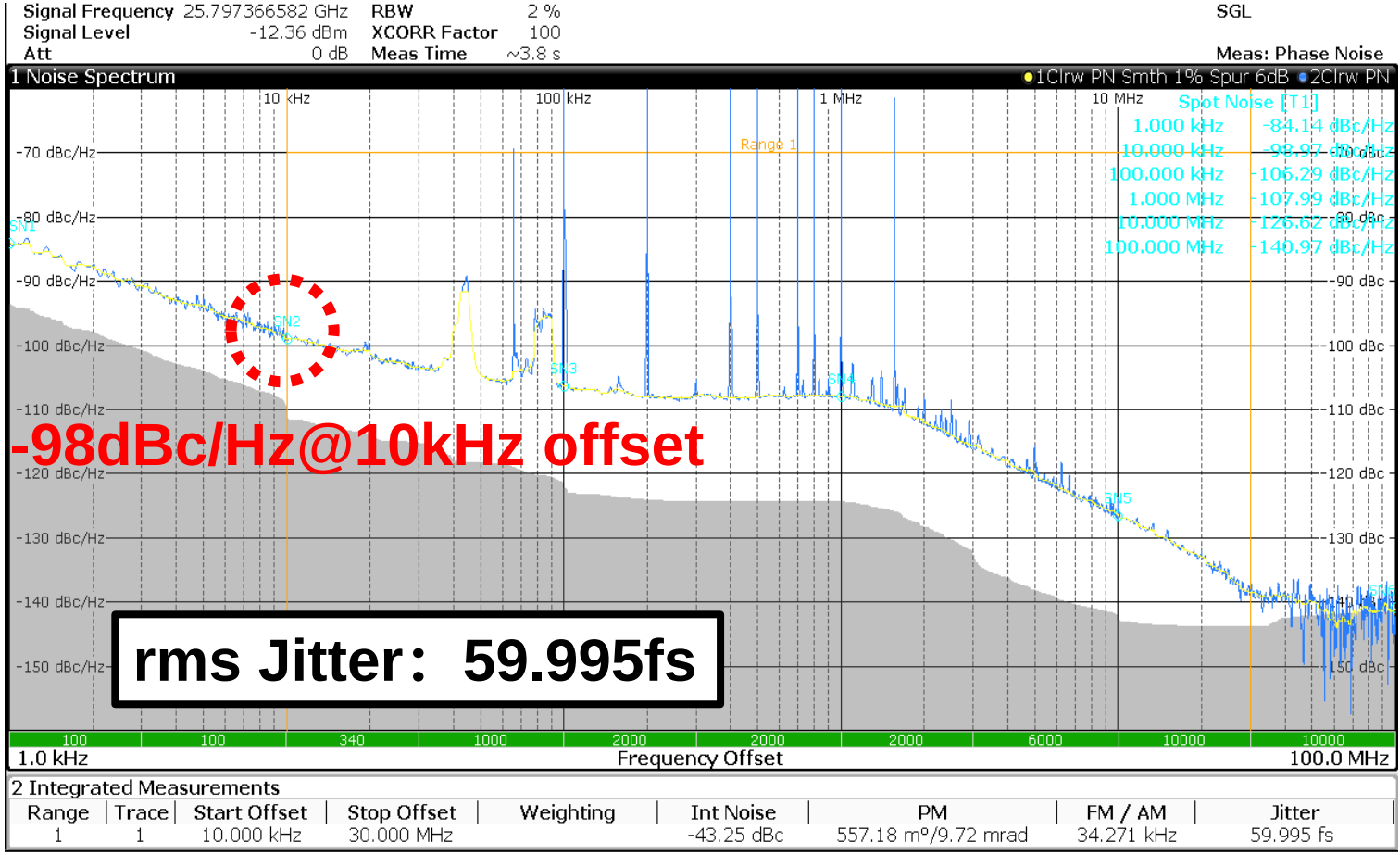


When TAPFD is OFF: in-band noise is dominated by charge pump

Measured Phase Noise



Measured PN w/ TAPFD in Charge



When TAPFD is ON: up to 24dB suppression of in-band phase noise

Power-Noise Tradeoff in CPPLL

Conventional PFD+CP	$\phi^2_{CP2REF,n} \propto \frac{1}{I_{CP}}$	2x Power -3dB PN
TAPFD+CP	$P_{TAPFD} = 1.07mw$ $P_{CP} = 0.82mw$	2.3x Power Up to -24dB PN

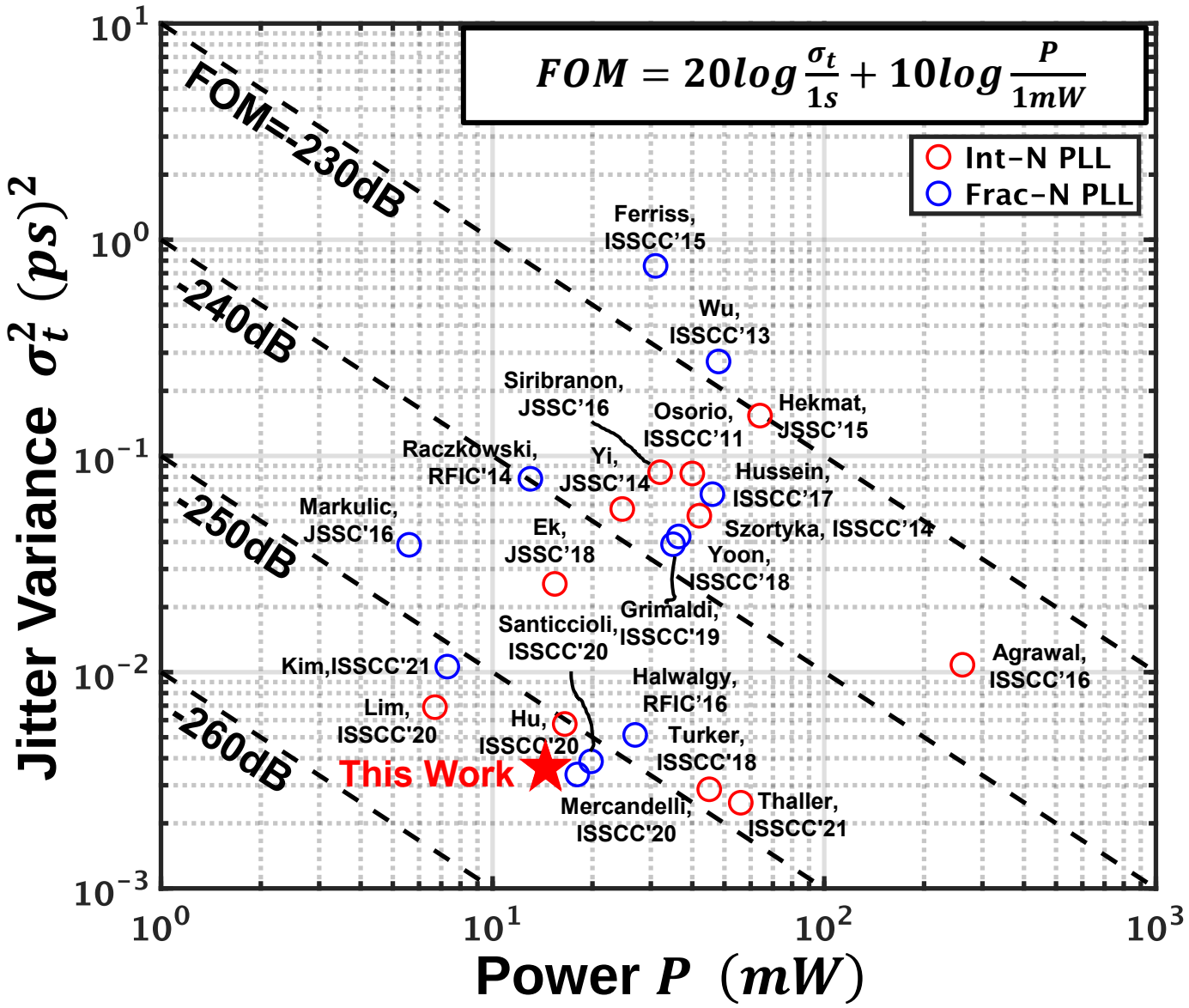
☺ The Power-Noise tradeoff in CP is broken by TAPFD

Performance Comparison

	This work	ISSCC'18[1] D. Turker	ISSCC'20[2] Y. Lim	ISSCC'21[3] E. Thaller	ISSCC'20[4] Y. Hu	VLSI'21 [8] Y. Zhao
Process	**65nm CMOS**	16nm FinFET	65nm CMOS	16nm FinFET	28nm LP CMOS	28nm CMOS
Architecture	**CPPLL w/ TAPFD**	CPPLL	Digital SSPLL	AD-SSPLL	Charge-Sharing Lock	Double Sampling
Type	**Integer-N**	Integer-N	Integer-N	Integer-N	Integer-N	Integer-N
Ref. Freq. [MHz]	**200**	500	50	245.76	250	250
Out. Freq. [GHz]	**24 to 28.2**	7.4 to 14	12.0 to 14.5	12.1 to 16.6	21.7 to 26.5	19
rms Jitter [fs]	**60@25.8GHz (10k to 30M)**	53.6 (10k to 10M)	83 (1k to 100M)	49.9 (1k to 100M)	75.9 (10k to 30M)	20.3 (10k to 100M)
Ref. Spur [dBc]	**-47**	-75.5	-75	-75.1	-45	-66
Core Area [mm²]	**0.45**	0.35	0.23	0.5	0.5	0.06
Power [mW]	**14.48**	45	6.7	56	16.5	12
FoM$_J$* [dB]	**-252.8**	-246.8	-253.0	-249.0	-250.2	-263

$*FoM_J = 10\log(jitter^2 \cdot Power/1mw)\ dB$

FoM of State-of-the-Art PLLs



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Conclusion

- **A 25.8GHz integer-N PLL is prototyped in 65nm CMOS, featuring:**
  - 60fs jitter, 14.48mW power and -252.8dB FoM_J
- **A time-amplifier based PFD is proposed:**
  - The power-noise tradeoff of CP is broken
  - Frequency detection capability is maintained for robust lock acquisition performance
- **Class-F VCO with built-in tripler:**
  - Better Q-factor for fundamental LC tank, thus better PN
  - Relax the operating frequency of divider